

**Western Digital®**

# **MK2 S5E BiCS5 512Gb iTLC -2/4/8D Micro Package SDSM PQ Report**

**MPNs:**

**SDSMGKLK2-128G**

**SDMMGKLK4-256G**

**SDSMGKLK8-512G**

WDC Packaging

7/1/2022

# PQ Full Qual - Matrix

Die Stack	Lots	Substrate vendor	EMI Tool
2D	Lot 1	Y	Tango
2D	Lot 2	Y	Linco
2D	Lot 3	Y	Tango
4D	Lot 1	X	Tango
4D	Lot 2	X	Linco
4D	Lot 3	X	Tango
8D	Lot 1	Y	Tango
8D	Lot 2	Y	Linco
8D	Lot 3	Y	Tango

**MK2 S5E BiCS5 512Gb iTLC - 2D**  
**9x13.3x0.87mm**  
**Shielded - 315 BGA**

# Dimension X-Y-Z, Warpage

## 2D (shielded)

Item	X(Width)	L(Length)	Package T w/o Bump	Pre-bump Height	Body T w/o Bump	Warpage @ RT
<b>Spec</b>	<b>9.0+/-0.05mm</b>	<b>13.3+/-0.05mm</b>	<b>Max. 0.87mm</b>	<b>50 +/-20um</b>	<b>0.770+/-0.025mm</b>	<b>[-30 um,75um]</b>
<b>Max</b>	8.996	13.299	0.796	53.000	0.766	30.0
<b>Min</b>	8.983	13.279	0.789	44.000	0.758	12.0
<b>Mean</b>	8.990	13.293	0.792	48.000	0.763	23.0
<b>Std Dev</b>	0.004	0.007	0.002	2.0	0.002	3.0

- Data taken from 60 units from 3 PQ lots (20 units/lot) and all dimensions within spec.

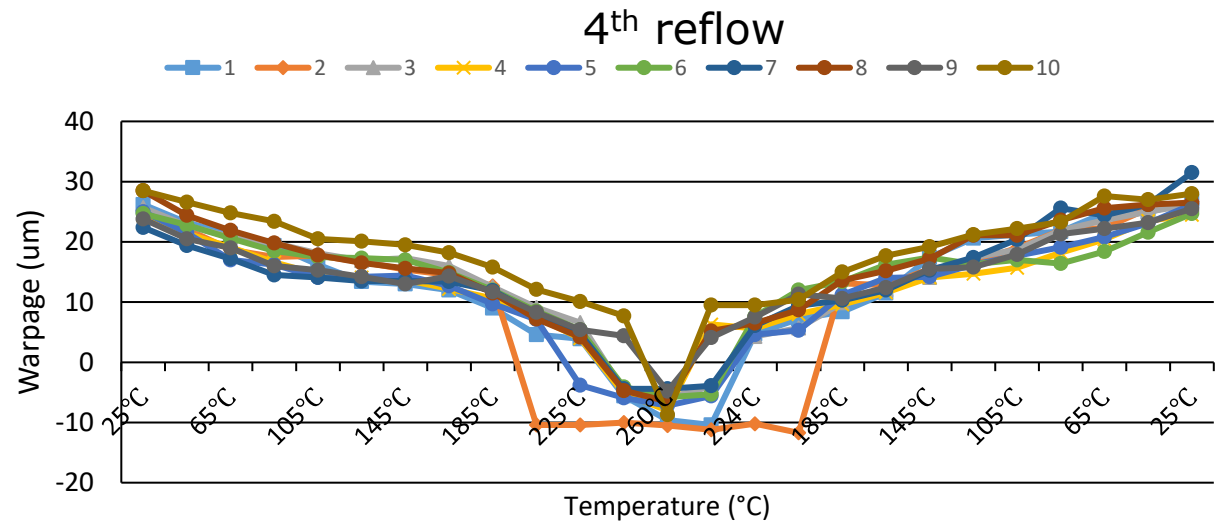
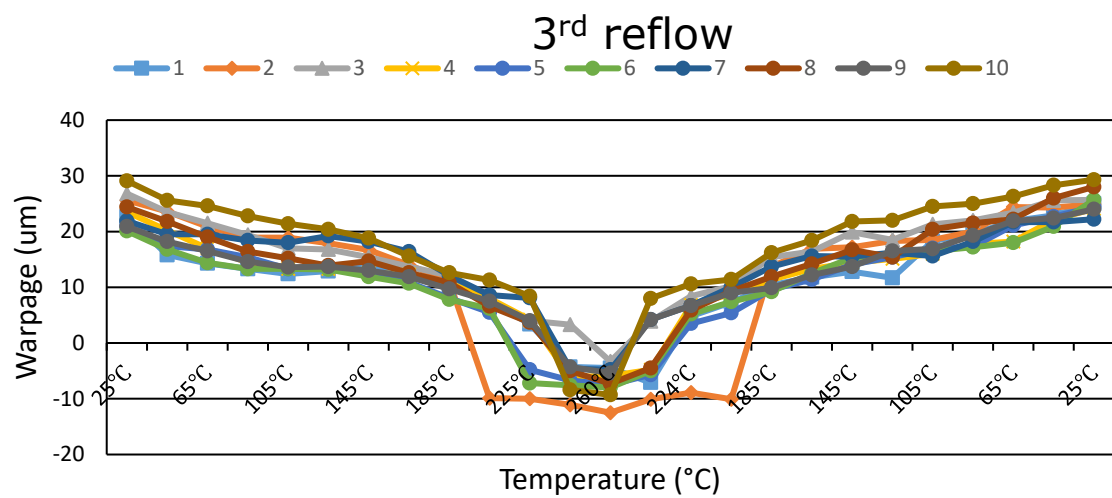
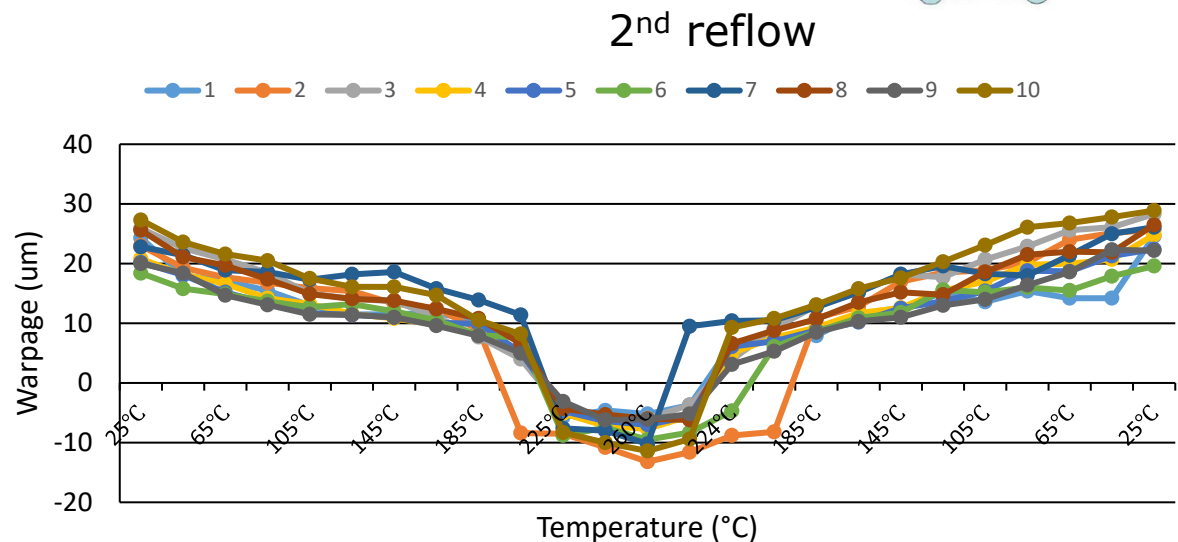
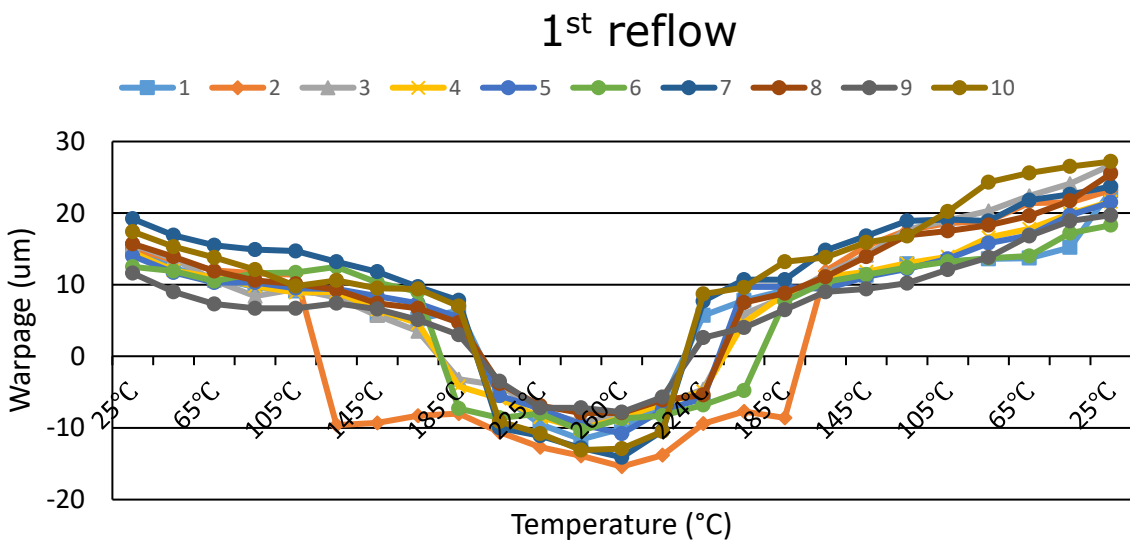
# Wire Bond Data (2D)

	Lot 1		Lot 2		Lot 3	
	Wire Pull	Ball Shear	Wire Pull	Ball Shear	Wire Pull	Ball Shear
<b>Spec (gf) – Min.</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>
<b>Max (gf)</b>	9.31	21.0	8.93	22.06	9.04	21.19
<b>Min (gf)</b>	6.10	17.0	6.42	17.86	6.09	17.58
<b>Avg (gf)</b>	7.64	19.17	7.54	19.62	7.47	19.45
<b>Std Dev (gf)</b>	0.66	0.80	0.51	0.95	0.57	0.78

- Data taken from 36 wires (5 units/lot) from 3 PQ lots and passed wire pull and bond shear.

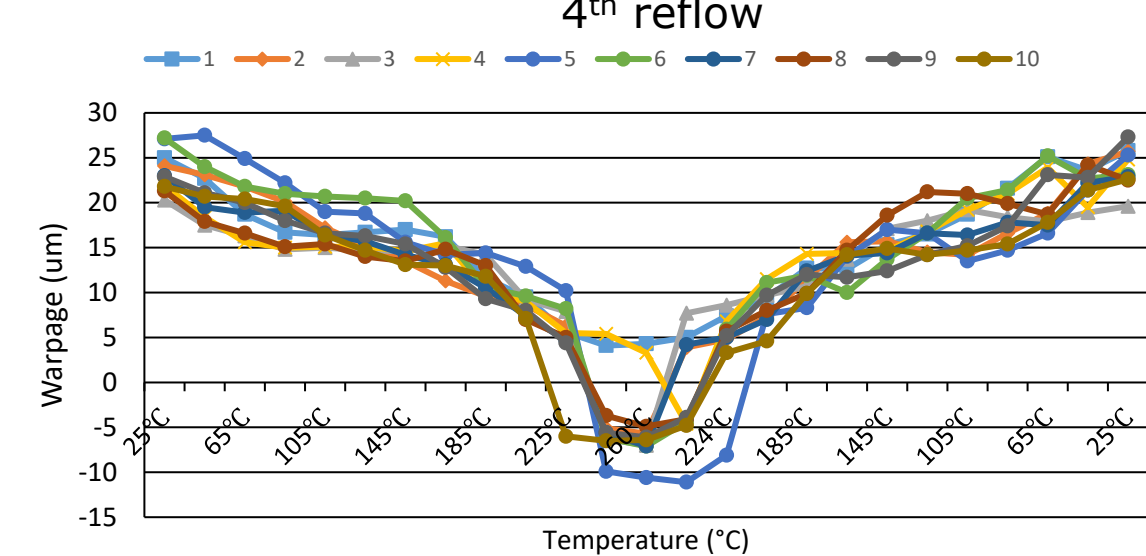
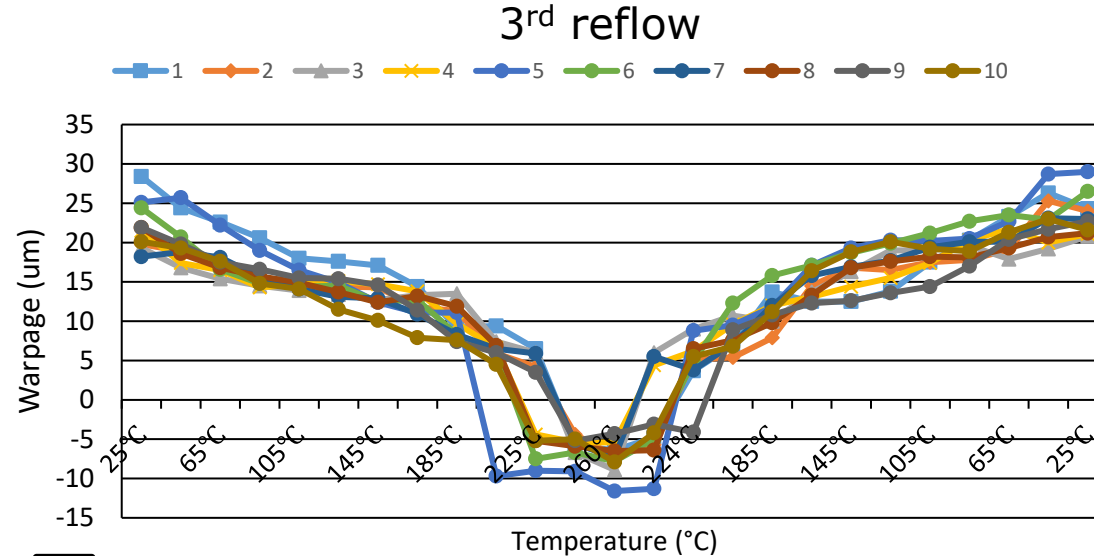
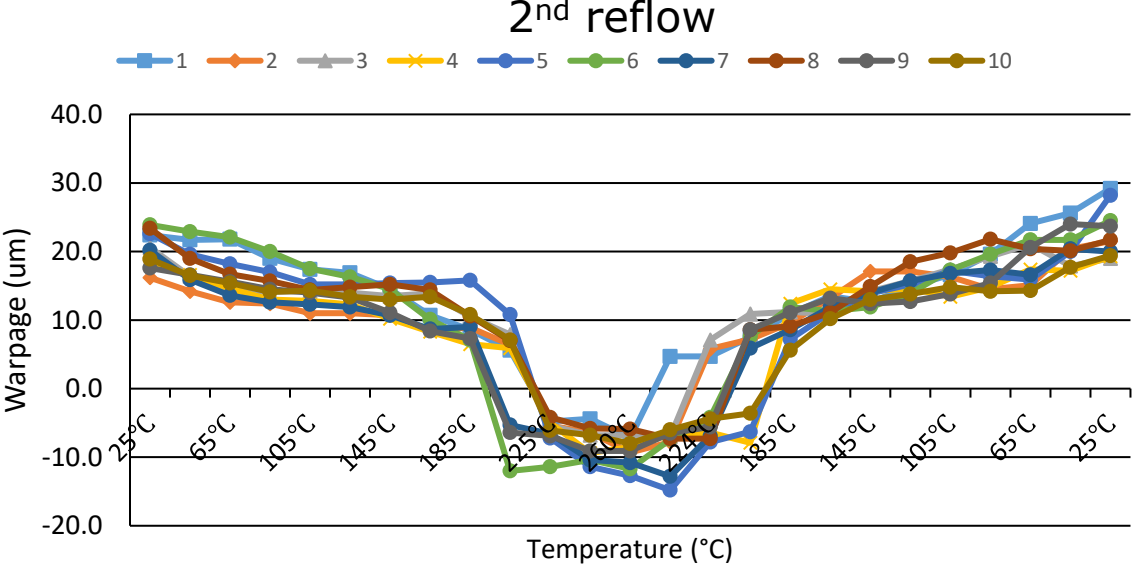
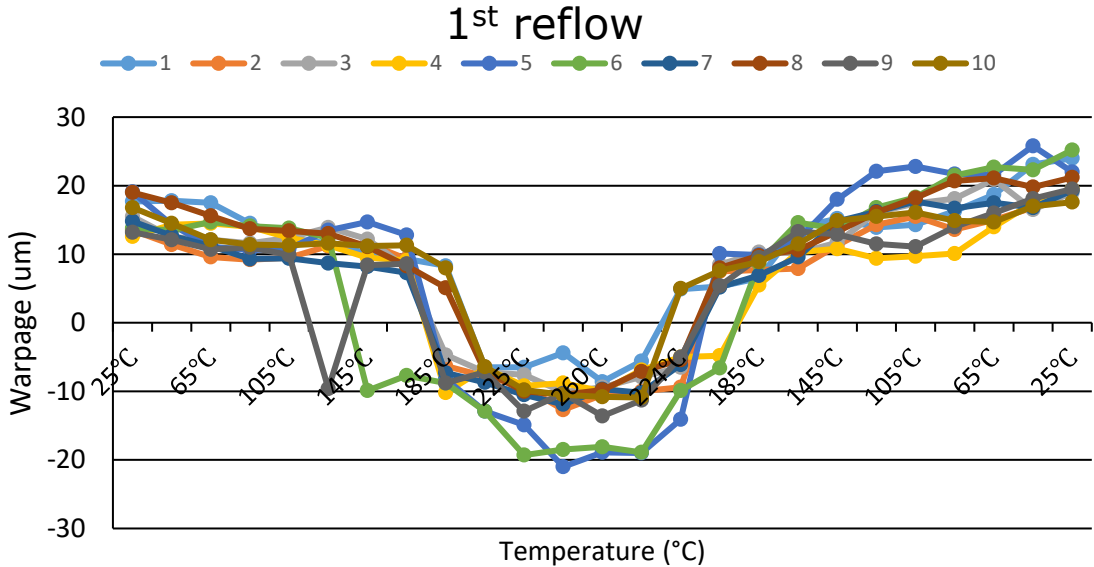
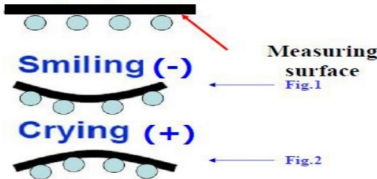
# Shadow Moiré (2D)

**Dry condition samples** - meets Apple spec for all temperature range specified



# Shadow Moiré (2D)

**Wet condition samples** - meets Apple spec for all temperature range specified



# Tape Adhesion test (2D)

20 units from each of 3 PQ lots

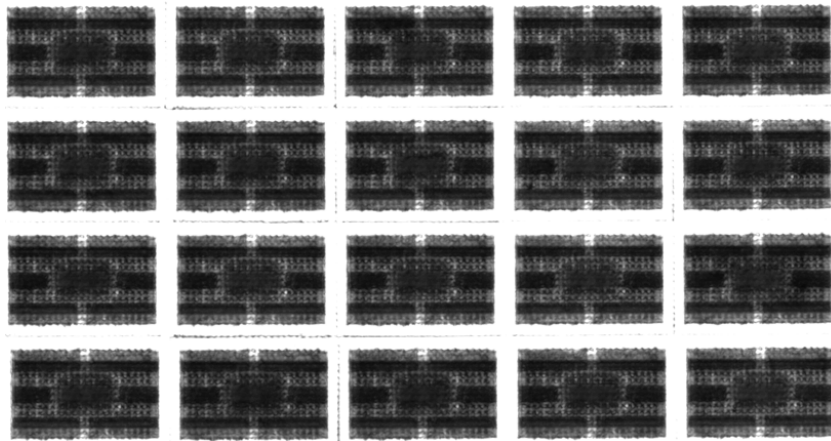
AI No.	Qty	Comment
Lot1	20	Peeling test pass 5B spec
Lot2	20	Peeling test pass 5B spec
Lot3	20	Peeling test pass 5B spec

Tape adhesion test done as per ASTM D-3359 at  $T_a = 25^\circ\text{C}$  and it meets peeling criterion  $\geq 4\text{B}$

# Contact Resistance and Delam check (2D)

Test	Pkg Type	Spec	Test result	Sample size	Remarks
Delamination check by CSAM	Shield	JED22-A113	0 fail / 60ea	60units	Require pre-conditioning with MSL level 3A and measure it after 260C 4x IR reflow
Contact Resistance check	Shield	<0.6Ω	0 fail / 60ea	60 units	

- Data taken from 60 units from 3 PQ lots (20 units/lot)
- CSAM image post MSL3A shows no failures.



# Package Reliability Data (2D) – Full Qual

## Package Qual Lot #1 (Substrate Vendor Y, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (2D) – Full Qual

## Package Qual Lot #2 (Substrate Vendor Y, EMI-Linco)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (2D) – Full Qual

## Package Qual Lot #3 (Substrate Vendor Y, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

**MK2 S5E BiCS5 512Gb iTLC - 4D**  
**9x13.3x0.87mm**  
**Shielded - 315 BGA**

# Dimension X-Y-Z, Warpage

## 4D (shielded)

Item	X(Width)	L(Length)	Package T w/o Bump	Pre-bump Height	Body T w/o Bump	Warpage @ RT
<b>Spec</b>	<b>9.0+/-0.05mm</b>	<b>13.3+/-0.05mm</b>	<b>Max. 0.87mm</b>	<b>50 +/-20um</b>	<b>0.770+/-0.025mm</b>	<b>[-30 um,75um]</b>
<b>Max</b>	8.996	13.298	0.808	52.000	0.764	44.0
<b>Min</b>	8.982	13.276	0.800	47.000	0.758	19.0
<b>Mean</b>	8.991	13.292	0.804	49.000	0.761	34.0
<b>Std Dev</b>	0.003	0.005	2.0	0.001	0.002	4.1

- Data taken from 60 units from 3 PQ lots (20 units/lot) and all dimensions within spec.

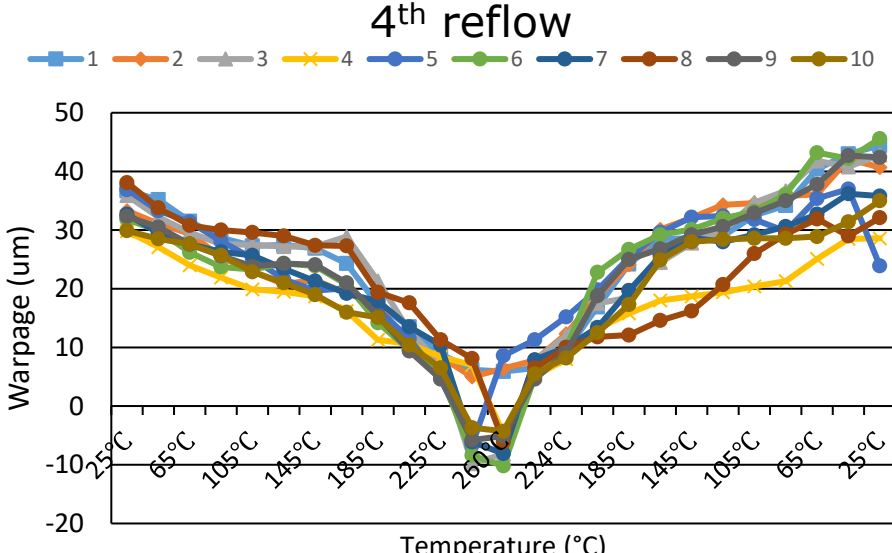
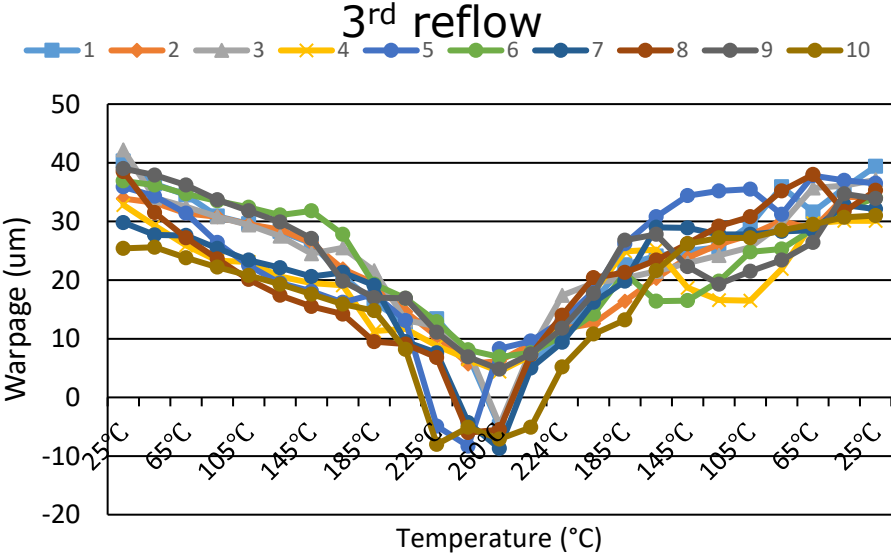
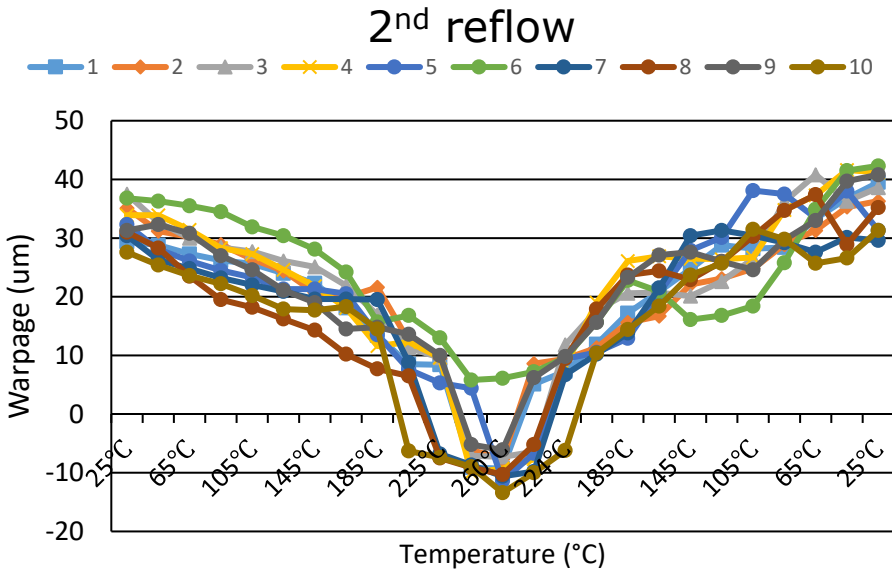
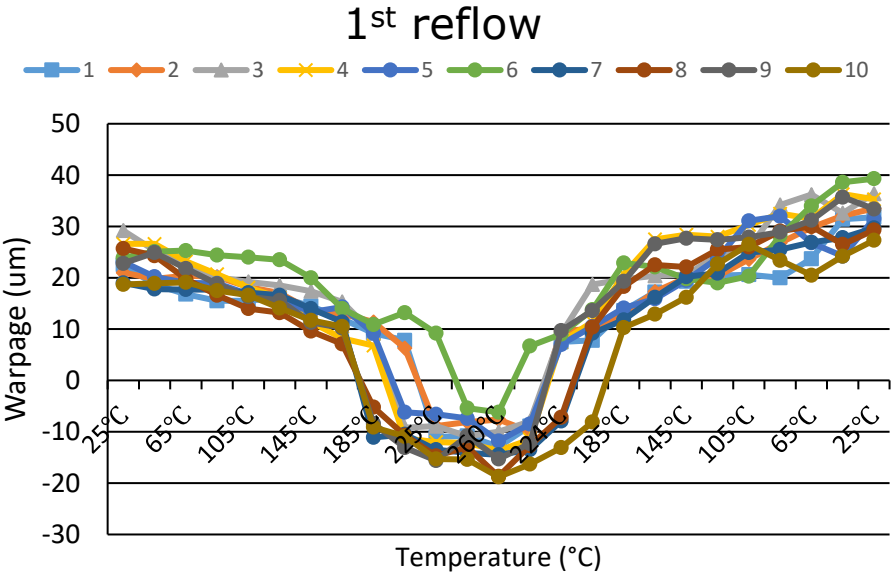
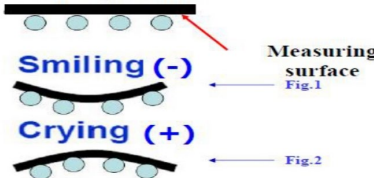
# Wire Bond Data (4D)

	Lot 1		Lot 2		Lot 3	
	Wire Pull	Ball Shear	Wire Pull	Ball Shear	Wire Pull	Ball Shear
<b>Spec (gf) – Min.</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>
<b>Max (gf)</b>	6.54	21.33	6.07	21.19	6.23	21.86
<b>Min (gf)</b>	3.85	17.86	3.75	18.06	3.48	17.35
<b>Avg (gf)</b>	4.89	19.46	4.84	19.64	4.78	19.55
<b>Std Dev (gf)</b>	0.47	0.74	0.44	0.60	0.46	0.76

- Data taken from 36 wires (5 units/lot) from 3 PQ lots and passed wire pull and bond shear.

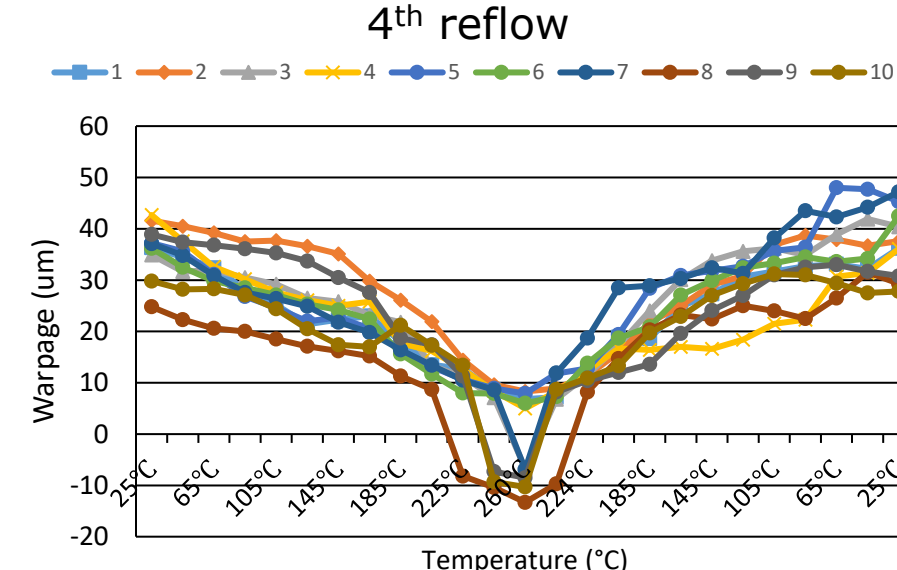
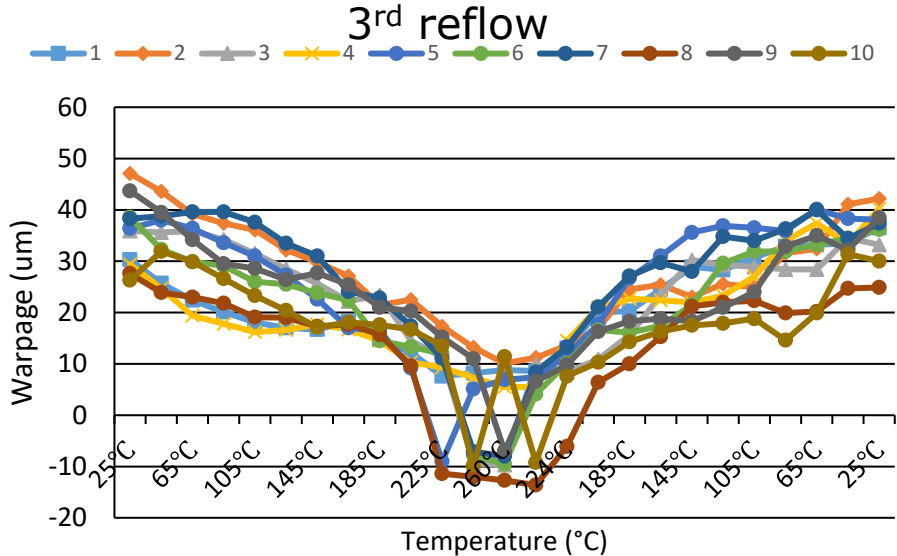
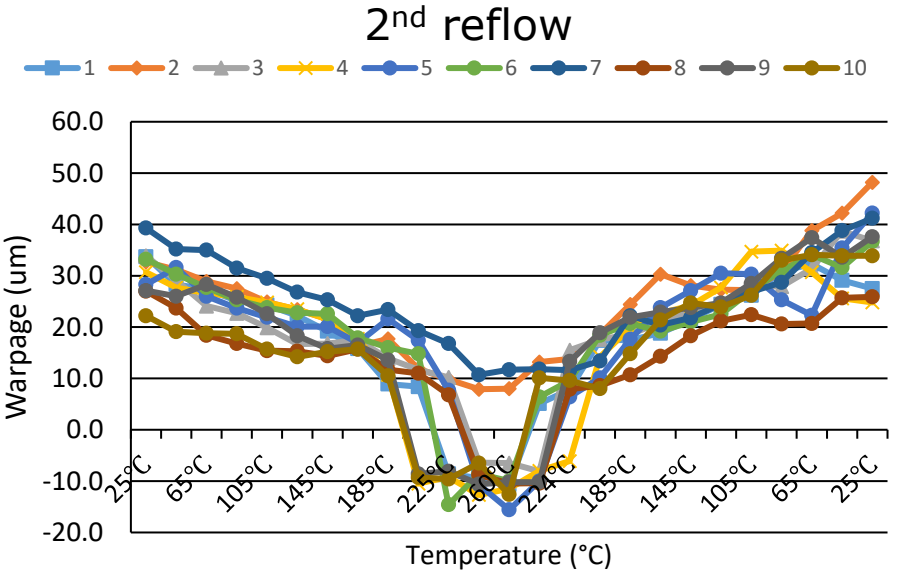
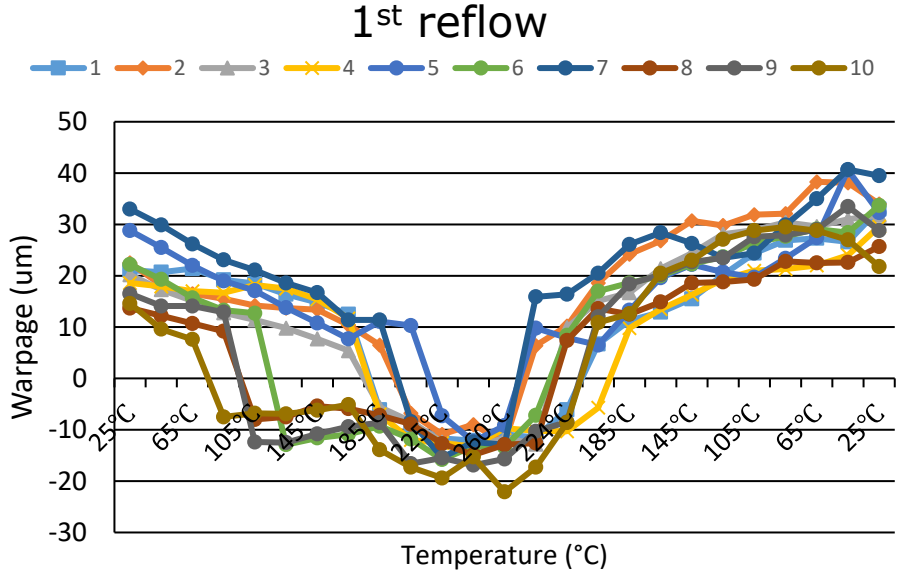
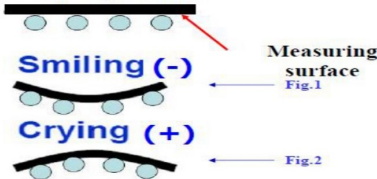
# Shadow Moiré (4D)

Dry condition samples - meets Apple spec for all temperature range specified



# Shadow Moiré (4D)

Wet condition samples - meets Apple spec for all temperature range specified



# Tape Adhesion test (4D)

20 units from each of 3 PQ lots

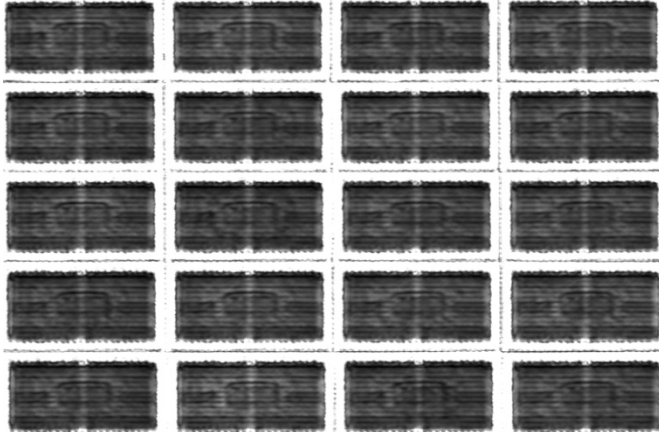
AI No.	Qty	Comment
Lot1	20	Peeling test pass 5B spec
Lot2	20	Peeling test pass 5B spec
Lot3	20	Peeling test pass 5B spec

Tape adhesion test done as per ASTM D-3359 at  $T_a = 25^\circ\text{C}$  and it meets peeling criterion  $\geq 4B$

# Contact Resistance and Delam check (4D)

Test	Pkg Type	Spec	Test result	Sample size	Remarks
Delamination check by CSAM	Shield	JED22-A113	0 fail / 60ea	60units	Require pre-conditioning with MSL level 3A and measure it after 260C 4x IR reflow
Contact Resistance check	Shield	<0.6Ω	0 fail / 60ea	60 units	

- Data taken from 60 units from 3 PQ lots (20 units/lot)
- CSAM image post MSL3A shows no failures



# Package Reliability Data (4D) – Full Qual

## Package Qual Lot #1 (Substrate Vendor X, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (4D) – Full Qual

## Package Qual Lot #2 (Substrate Vendor X, EMI-Linco)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (4D) – Full Qual

## Package Qual Lot #3 (Substrate Vendor X, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

**MK2 S5E BiCS5 512Gb iTLC - 8D**  
**9x13.3x0.9mm**  
**Shielded - 315 BGA**

# Dimension X-Y-Z, Warpage

## 8D (shielded)

Item	X(Width)	L(Length)	Package T w/o Bump	Pre-bump Height	Body T w/o Bump	Warpage @ RT
<b>Spec</b>	<b>9.0+/-0.05mm</b>	<b>13.3+/-0.05mm</b>	<b>Max. 0.90mm</b>	<b>50 +/-20um</b>	<b>0.800+/-0.025mm</b>	<b>[-30 um,75um]</b>
<b>Max</b>	8.993	13.283	0.838	56.000	0.796	41.000
<b>Min</b>	8.980	13.263	0.828	48.000	0.791	23.000
<b>Mean</b>	8.987	13.278	0.833	53.000	0.793	36.000
<b>Std Dev</b>	0.003	0.005	0.005	2.0	0.002	3.0

- Data taken from 60 units from 3 PQ lots (20 units/lot) and all dimensions within spec.

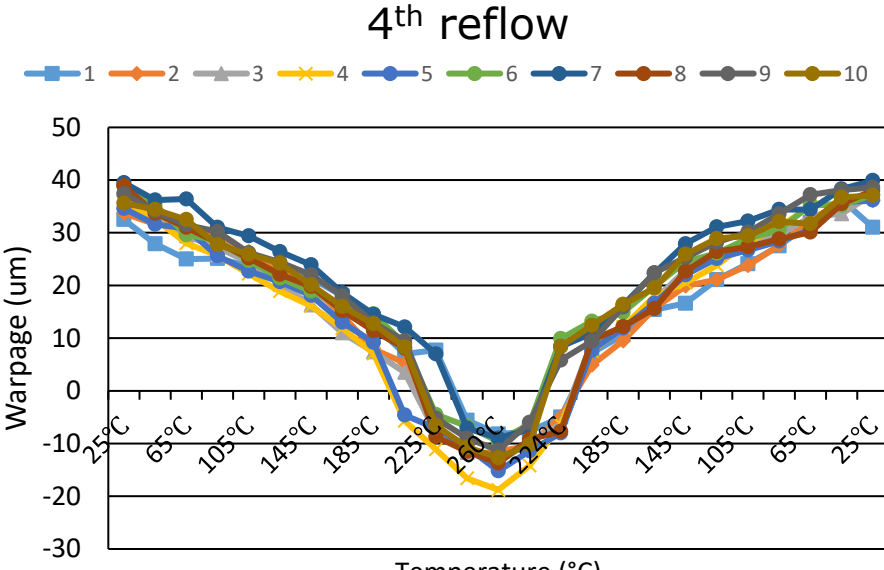
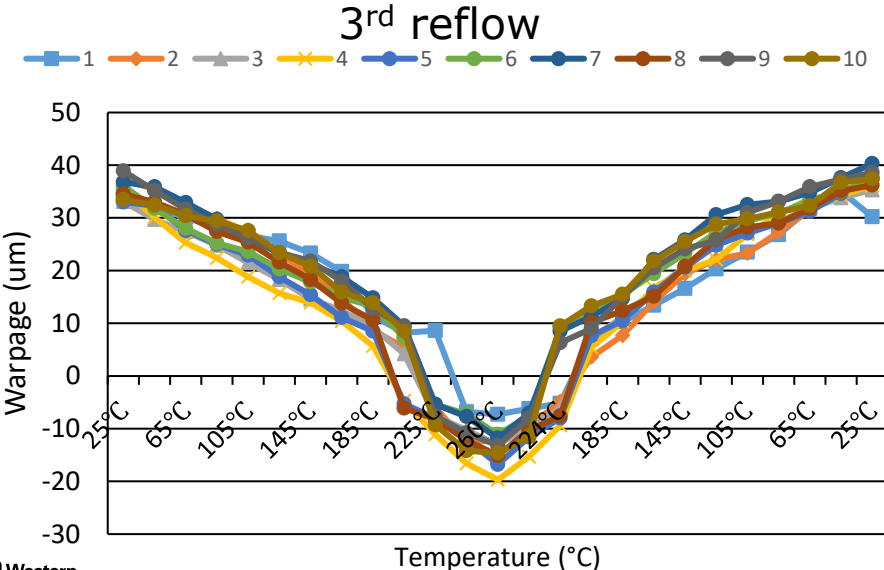
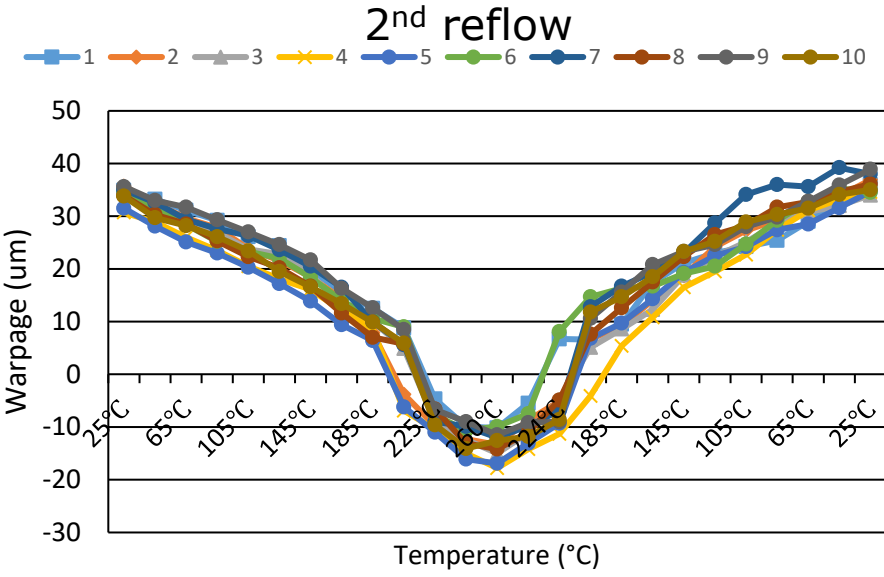
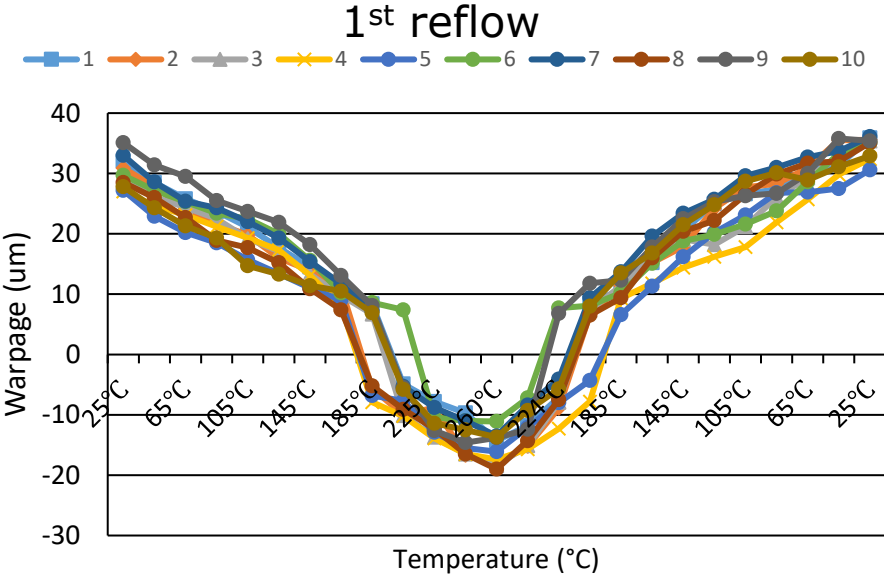
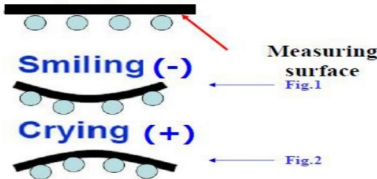
# Wire Bond Data (8D)

	Lot 1		Lot 2		Lot 3	
	Wire Pull	Ball Shear	Wire Pull	Ball Shear	Wire Pull	Ball Shear
<b>Spec (gf) – Min.</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>	<b>1.8</b>	<b>10</b>
<b>Max (gf)</b>	6.79	20.35	6.93	20.39	6.53	20.34
<b>Min (gf)</b>	4.42	17.40	4.30	17.35	3.81	16.69
<b>Avg (gf)</b>	5.50	18.90	5.62	18.92	5.45	18.86
<b>Std Dev (gf)</b>	0.46	0.53	0.50	0.54	0.53	0.58

- Data taken from 36 wires (5 units/lot) from 3 PQ lots and passed wire pull and bond shear.

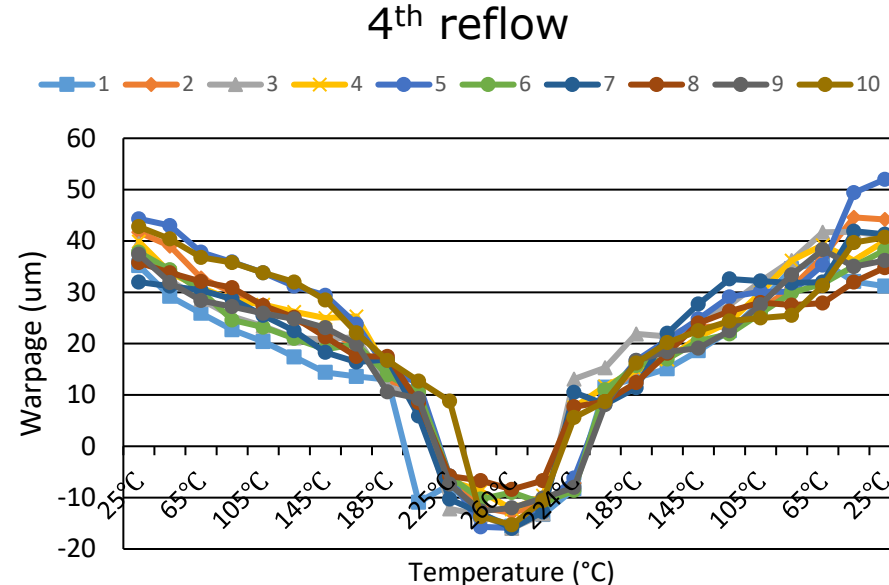
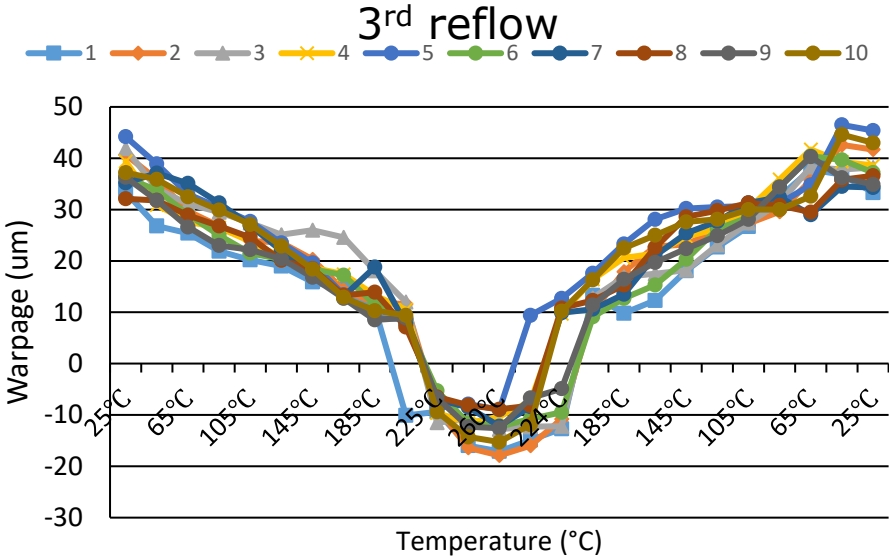
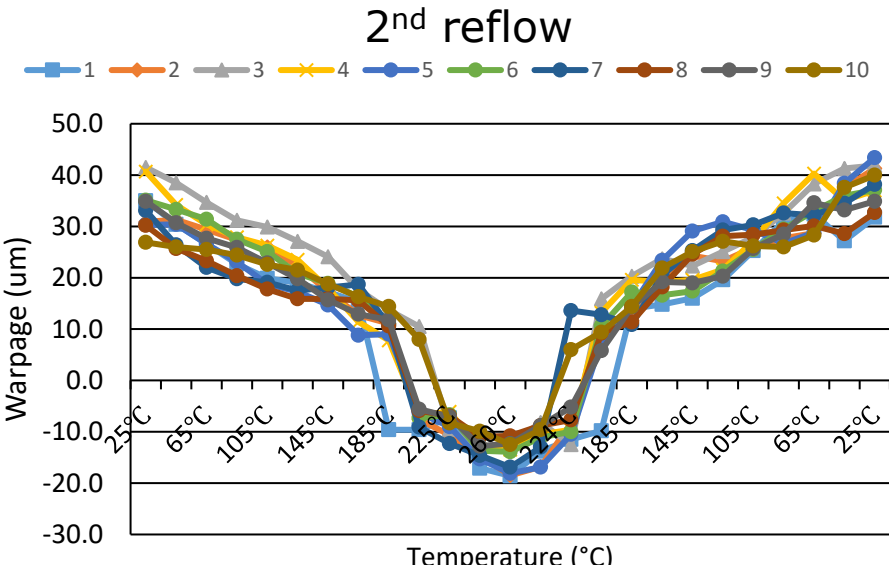
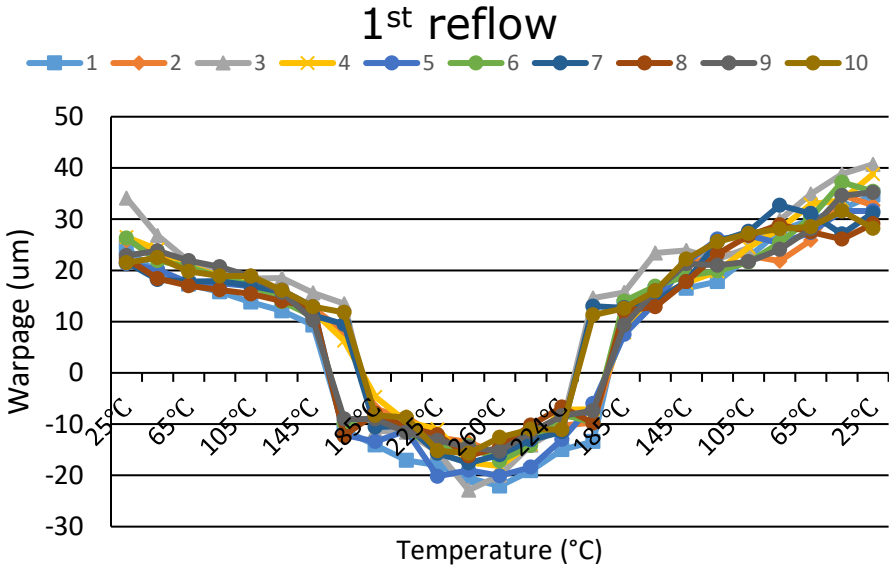
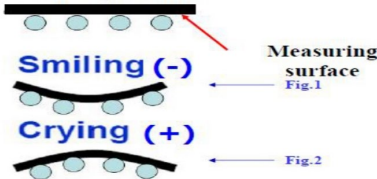
# Shadow Moiré (8D)

Dry condition samples - meets Apple spec for all temperature range specified



# Shadow Moiré (8D)

Wet condition samples - meets Apple spec for all temperature range specified



# Tape Adhesion test (8D)

20 units from each of 3 PQ lots

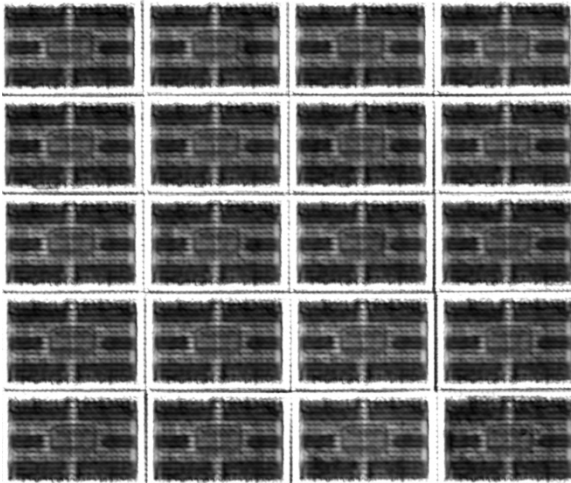
AI No.	Qty	Comment
Lot1	20	Peeling test pass 5B spec
Lot2	20	Peeling test pass 5B spec
Lot3	20	Peeling test pass 5B spec

Tape adhesion test done as per ASTM D-3359 at  $T_a = 25^\circ\text{C}$  and it meets peeling criterion  $\geq 4\text{B}$

# Contact Resistance and Delam check (8D)

Test	Pkg Type	Spec	Test result	Sample size	Remarks
Delamination check by CSAM	Shield	JED22-A113	0 fail / 60ea	60units	Require pre-conditioning with MSL level 3A and measure it after 260C 4x IR reflow
Contact Resistance check	Shield	<0.6Ω	0 fail / 60ea	60 units	

- Data taken from 60 units from 3 PQ lots. (20 units/lot)
- CSAM image post MSL3A shows no failures.



# Package Reliability Data (8D) – Full Qual

## Package Qual Lot #1 (Substrate Vendor X, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (8D) – Full Qual

## Package Qual Lot #2 (Substrate Vendor X, EMI-Linco)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# Package Reliability Data (8D) – Full Qual


## Package Qual Lot #3 (Substrate Vendor X, EMI-Tango)

Test Items	Sample Size (ea)	Test Condition	Criteria	Intermediate read-point	Result
Pre-condition: MSL3A +4xIR	280	60° C; 60% RH; 40hours 4xIR.	No Failure	SAT result	0/280
				Test result	0/280
TMCL for embedded components after pre-con (Temperature Cycling Test)	77	-55°C to 125°C; 300cycles	No Failure	After 300cys	0/77
		-55°C to 125°C; 500cycles	No Failure	After 500cys	0/77
		-55°C to 125°C; 700cycles	No Failure	After 700cys	0/77
Biased-HAST after pre-con (Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 3.6V/1.95V/0.99V for 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 3.6V/1.95V/0.99V for 264hours.	No Failure	After 264hrs	0/77
Un-Biased-HAST after pre-con (Un-Biased Highly Accelerated Stress Test)	77	110°C, 85%RH; 96hours.	No Failure	After 96hrs	0/77
		110°C, 85% RH; 264hours.	No Failure	After 264hrs	0/77
HTST after pre-con (High Temperature Storage Test)	45	150°C; 300hours	No Failure	After 300hrs	0/45
		150°C; 500hours	No Failure	After 500hrs	0/45

# MCP ESD CDM (500V, 400V, 250V) Results

<b>BiCS5 512Gb iTLC S5E – 2D</b>	<b>Sample size (ea)</b>	<b>Results</b>
500V CDM	10	0F/10T
400V CDM	10	0F/10T
250V CDM	10	0F/10T
<b>BiCS5 512Gb iTLC S5E – 4D</b>	<b>Sample size (ea)</b>	<b>Results</b>
500V CDM	10	0F/10T
400V CDM	10	0F/10T
250V CDM	10	0F/10T
<b>BiCS5 512Gb iTLC S5E – 8D</b>	<b>Sample size (ea)</b>	<b>Results</b>
500V CDM	10	0F/10T
400V CDM	10	0F/10T
250V CDM	10	0F/10T

- All die stacks passed ESD min. spec  $\geq$  250V.

The image features the Western Digital logo in white, bold, sans-serif font, centered horizontally. The background is a dark, abstract composition of overlapping, semi-transparent brushstrokes in shades of orange, red, and teal, creating a sense of motion and depth. The logo is the primary focus, with a registered trademark symbol (®) at the end.

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