S5E+BiCS FLASH™ Gen5 (BiCS5) Improved TLC3 (iTLC3) Mk2 MCP Technical Data Sheet

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1 Introduction

1.1 General Description

The devices listed in Table 1 are Kioxia S5E+BiCS5 MCP Electrically Erasable and Programmable Read-Only Memory (E²PROM) of 64Gbytes, 128Gbytes, 256Gbytes, 512Gbytes and 1Tbytes.

These devices are composed of BiCS5 512Gbits TLC 2plane Die, and these TLC (3bit per cell) devices are supposed to be operated with TLC mode. Here it is allowed to use these devices with SLC (1bit per cell)/TLC mixed condition and the density and capacity of them is depend on the ratio of usage between SLC and TLC in a device. Then the density and capacity is defined by the size based on logical address area with TLC 100% usage mode in this document. As for the restrictions, conditions and reliability related to SLC/TLC mixed usage, please refer to the chapter of 2.2 Reliability of Internal Raw NAND.

A Kioxia S5E+BiCS5 MCP device includes:

- A S5E Controller
- One or more BiCS5 512Gb TLC 2plan dies
- One lane of PCIe interface
- Hardware (HW) bypass, SPI, and JTAG interfaces only for KIOXIA's internal test purpose.

Operational Firmware (FW) is installed in Kioxia S5E MCP NAND device, and the operation of the FW is guaranteed by S5E Controller Supplier.

Note: The Memory density to the number of DP is rounded down to the nearest integer in this document.

- BiCS5 512Gb TLC 2plane die

  64 GBytes indicates the rounding result of calculation of (512Gbits/8bits) *1DP.

  128 GBytes indicates the rounding result of calculation of (512Gbits/8bits) *2DP.

  256 GBytes indicates the rounding result of calculation of (512Gbits/8bits) *4DP.

  512 GBytes indicates the rounding result of calculation of (512Gbits/8bits) *8DP.

  1024 GBytes indicates the rounding result of calculation of (512Gbits/8bits) *16DP.

*DP is short for Die stacked Package. And the notation of "nDP" means # of die stack.

1.2 Definitions and Abbreviations

This chapter defines terminologies and abbreviations used across this document.

- ANI: Apple NAND Interface between S5E controller and BiCS5 raw NAND
- ASI: Apple Storage Interface
- ASPM: Active State Power Management. Power management protocol of PCIe.
- P/E: Program / Erase
- SOL: Start Of Life. It is initial device status at shipment from Kioxia.
- EOL: End Of Life. It is device status at maximum program/erase cycles which is defined by Endurance P/E cycles in Chapter 2.2
- EFR: Early Failure Rate. Failure rate up to 10% of EOL P/E cycles in Chapter 2.2.
- PTS: Production Test System (A test program provided by Apple and run by KIOXIA as a part of KIOXIA outgoing test)
- S5E: Memory controller designed by Apple
- S5E Controller Supplier: Apple
- TCM: Test Coverage Matrix
- GBB(s): Grown Bad block(s)
- ESF: Erase Status Failure
- PSF: Program Status Failure
- UECC: Uncorrectable ECC. Uncorrectable read error.
- Verify-UECC: UECC occurring during the 1st block read which is performed immediately after full block program completion.
- Latent-UECC: UECC occurring during any other (non-verify) read
- DPPM: Defective Parts Per Million
- Shall: The term “shall” describes mandatory item
- Should: The term “should” describes optional item
- SLC 1P0V: 1 Program pulse 0 Verify that is SLC program without verify mode

1.3 Parts Number

Table 1 Kioxia S5E+BiCS5 MCP device Part Number List

Part Number for MP (15digit)	Part Number for Qual (16digit)	NAND Die	DP	Package Type	Wafer Fab	Substrate Type	Assembly Fab
THGBY8G9A15LFAN	THGBY8G9A15LFAN1	BiCS5 512Gbits TLC 2plane	1	Micro Package Type 1	YOK	X	PTI
	THGBY8G9A15LFANB					Y	AMK (*1)
	THGBY8G9A15LFANC						AMK (*2)
	THGBY8G9A15LFANK				KIW	X	PTI
	THGBY8G9A15LFANS					Y	AMK (*1)
	THGBY8G9A15LFANT						AMK (*2)
THGBY8T0A25LFAN	THGBY8T0A25LFAN1		2		YOK	X	PTI
	THGBY8T0A25LFANB					Y	AMK (*1)
	THGBY8T0A25LFANC						AMK (*2)
	THGBY8T0A25LFANK				KIW	X	PTI
	THGBY8T0A25LFANS					Y	AMK (*1)
	THGBY8T0A25LFANT						AMK (*2)
THGBY8T1A45LFAN	THGBY8T1A45LFAN1		4		YOK	X	PTI
	THGBY8T1A45LFANB					Y	AMK (*1)
	THGBY8T1A45LFANC						AMK (*2)
	THGBY8T1A45LFANK				KIW	X	PTI
	THGBY8T1A45LFANS					Y	AMK (*1)
	THGBY8T1A45LFANT						AMK (*2)
THGBY8T2A85LFAN	THGBY8T2A85LFAN1		8	Micro Package Type 2	YOK	X	PTI
	THGBY8T2A85LFANB					Y	AMK (*1)
	THGBY8T2A85LFANC						AMK (*2)
	THGBY8T2A85LFANK				KIW	X	PTI
	THGBY8T2A85LFANS					Y	AMK (*1)
	THGBY8T2A85LFANT						AMK (*2)
THGBY8T3AB5LFAP	THGBY8T3AB5LFAPB		16	Mini Package	YOK	Y	YOK

(*1) AMK assembly parts with HA6 Au wire (non POR)

(*2) AMK assembly parts with AT2 Au wire (POR)

Table 2 Relation between Apple Part Number (APN) and Kioxia Part Number

APN	Engineering Configuration Code	Part Number for MP (15digit)	Part Number for Qual (16digit)
335S00542	1260	THGBY8G9A15LFAN	THGBY8G9A15LFAN1
			THGBY8G9A15LFANB
			THGBY8G9A15LFANC
			THGBY8G9A15LFANK
			THGBY8G9A15LFANS
			THGBY8G9A15LFANT
335S00551	1265	THGBY8T0A25LFAN	THGBY8T0A25LFAN1
			THGBY8T0A25LFANB
			THGBY8T0A25LFANC
			THGBY8T0A25LFANK
			THGBY8T0A25LFANS
			THGBY8T0A25LFANT
335S00552	1266	THGBY8T1A45LFAN	THGBY8T1A45LFAN1
			THGBY8T1A45LFANB
			THGBY8T1A45LFANC
			THGBY8T1A45LFANK
			THGBY8T1A45LFANS
			THGBY8T1A45LFANT
335S00553	1267	THGBY8T2A85LFAN	THGBY8T2A85LFAN1
			THGBY8T2A85LFANB
			THGBY8T2A85LFANC
			THGBY8T2A85LFANK
			THGBY8T2A85LFANS
			THGBY8T2A85LFANT
335S00561	17M2	THGBY8T3AB5LFAP	THGBY8T3AB5LFAPB

1.4 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VDD	Controller digital logic power supply voltage	0 to 0.96	V
VCCQ_IO	Controller IO voltage	0 to 1.95 0 to 1.3	V
VCCQ_ANI	ANI voltage	0 to 1.3	V
VQPS (*1)	Fuse burn supply voltage	0 to 1.85	V
VCC	Raw NAND power supply voltage	-0.6 to 4.6	V
VPP (*2)	Raw NAND power supply voltage	0 to 16	V
V_{IN} (VDDIO=1.8V)	Input voltage for S5E Controller	-0.3 to 1.95	V
V_{IN} (VDDIO=1.23V)		-0.3 to 1.3	V
V_{IN} (VCCQ_ANI=1.23V)	Input voltage for Internal raw NAND (WP_N pin)	-0.2 to 1.5	V
T_{SOLDER}	Soldering temperature	240	°C
T_{STR}	Storage temperature	-15 to 85	°C
T_{OPR}	Operating Temperature	-15 to 85	°C

(*1) VQPS shall be tied to 1.8V only for fuses burn. For all other uses pin shall be connected to GND.

(*2) S5E+BiCS5 MCP device doesn't support VPP function.

1.5 Recommended Operating Conditions

Table 4 and Table 5 show operation modes and recommended operation conditions for S5E+BiCS5 MCP device, respectively.

Table 4 Operation Modes

Operation Mode	VDD [V]	VccQ_IO [V]	VccQ_ANI [V]	VCC [V]	BCM_N	PCIe Gen	ANI Frequency [MHz]
1	0.9	1.8	1.23	2.5	"0"	3	266/600
2	0.835	1.23	1.23	2.5	"1"	4	600

[Note] BCM_N (EXT_DQS) pin is used as a bootstrap for indicating IO supplies voltage for S5E controller.

Table 5 Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Notes
VCCQ_IO (*1)	1.7	1.8	1.95	V	High VCCQ_IO operation mode
	1.14	1.23	1.3	V	Low VCCQ_IO operation mode
VCCQ_ANI (*1)	1.14	1.23	1.3	V	Low VCCQ_ANI operation mode
VQPS	Connected to GND			V	Fuse burn supply voltage
VDD (*1)	0.845	0.9	0.94	V	High VDD operation mode
	0.78	0.835	0.9	V	Low VDD operation mode
VCC	2.35	N/A	2.75	V	VCC rail is supplying NAND dies only
VPP(*2)	Opened or connected to GND			V	VPP rail is supplying NAND dies only
T_{CASE}	-15	N/A	85	°C	MCP Package surface temperature

(*1) PTS is performed at typical voltage for VDD, VCCQ_IO and VCCQ_ANI according to an instruction of S5E Controller Supplier. Other tests over Operational FW are performed at min / max voltage for VDD, VCCQ_IO and VCCQ_ANI.

(*2) Kioxia S5E+BiCS5 MCP device doesn't support VPP function.

1.6 PCIe Interface Feature

PCIe interface is configurable as either Gen1 x1, Gen2 x1, Gen3 x1 or Gen4 x1.

Note: PCIe interface is used in KIOXIA's outgoing test. However, PCIe function itself is guaranteed by S5E Controller Supplier.

1.7 Test Interfaces

Kioxia S5E+BiCS5 MCP device is comprised of the following interfaces.

- Hardware Bypass Mode Interface
- SPI Interface
- JTAG Interface

[Note]: These interfaces are used only for Kioxia's internal test purpose. Kioxia S5E+BiCS5 MCP device does not support the functionality of these test interfaces.

[Note]: As for detailed description of each test interface, please refer to Chapter 3 in "S5E Vendor Product Specification".

1.8 Controller HW & FW Version

Table 6 Controller HW & FW Version

KIOXIA's Part Number	Memory Die Type	DP	Controller HW Version	FW Version
THGBY8G9A15LFAN*	BiCS5 512Gb iTLC3	1	A1	11.0
THGBY8T0A25LFAN*		2	A1	11.0
THGBY8T1A45LFAN*		4	A1	11.0
THGBY8T2A85LFAN*		8	A1	11.0.1
THGBY8T3AB5LFAP*		16	A1	11.0

* means a single character variable that shall be given a specific value

[Note] Both Production FW (PFW) and Operational FW (OFW) are used in KIOXIA outgoing test, and OFW is deleted before shipping from KIOXIA. The operation of those FWs are guaranteed by S5E Controller Supplier.

2 Internal Raw NAND Key Features

This chapter describes the internal raw NAND die key features.

2.1 Internal Raw NAND Organization

Table 7 Internal Raw NAND Key Organization

Item	BiCS5 512Gb iTLC3	Unit
Page size	18,336	Bytes
Number of pages per block	1,344	Pages
Block size	21M	Bytes
Max number of Blocks	1,662	Blocks
Number of plane per die	2	Planes

2.2 Reliability of Internal Raw NAND

Table 8 Reliability of Internal Raw NAND

Item	BiCS5 512Gb iTLC3	Unit
SLC Endurance	100,000	P/E cycles
TLC Endurance	3,000	P/E cycles
Power Cycling Endurance	10,000,000	VCC ON/OFF cycles
Boot Block Endurance	100	P/E cycles

[Note] These reliability specifications cannot be guaranteed for all shipment Kioxia S5E+BiCS5 MCP devices because Kioxia S5E+BiCS5 MCP devices may have a damage by those endurance tests. Therefore, those specifications are evaluated by sampling and are guaranteed with average failure rate.

Kioxia S5E+BiCS5 MCP device does not allow to use SLC more than 15% of full media which is Apple's definition.

If a block is used by SLC/TLC mix mode, TLC endurance specification shall be applied.

2.3 Quality of Internal Raw NAND

Table 9 Quality of Internal Raw NAND

Cell Mode	P/E cycle Condition	Allowable Cumulative Failure Rate		
		Beyond allowable GBBs (*1)	Uncorrectable Data Loss classified as fatal error events (*2)	Caused by any defects in peripheral circuits
SLC TLC Total	30 P/E Cycle	200 ppm/die	50 ppm/die	
	EFR (*3)	1,000 ppm/die	100 ppm/die	
	100% of supported endurance (EOL)	300 ppm/die	300 ppm/die	

(*1) This valid block specification is defined in Table 10.

(*2) Uncorrectable fatal error events are classified in Table 11 and Table 12.

(*3) BiCS5 512Gb TLC die : 300 P/E Cycle for TLC and 10,000 P/E Cycle for SLC

[Note] These 30 P/E cycle / EFR / EOL failure rate specifications cannot be guaranteed for all shipment Kioxia S5E+BiCS5 MCP devices because Kioxia S5E+BiCS5 MCP devices may have a damage by 30 P/E cycle / EFR / EOL tests. Therefore, those specifications are evaluated by sampling and are guaranteed with average failure rate.

Table 10 Allowable GBBs for Internal Raw NAND

Item	BiCS Die Type	Cell Mode	30 P/E Cycle	10% of supported Endurance (EFR)	100% of supported Endurance (EOL)	Unit
Maximum GBBs	BiCS5 512Gb iTLC3	TLC	1	2	16	Blocks/die
		SLC	1	2	20% of tested blocks	Blocks/die

Table 11 Data Loss Classification for TLC and SLC 1P1V mode

Event	# of failing WLs		Classification
	Failing plane	Any adjacent plane	
ESF	-	-	ESF
PSF	Any	0-2 (*1)	PSF – Correctable
	> 1	> 1	PSF – Uncorrectable
Verify-UECC	Any (Detectable(*2))	0	Time zero – Correctable
	0-2 (Sequential)	0	
	> 0	> 0	Time zero – Uncorrectable
Latent-UECC	1	0	Latent – Correctable
	Any other case		Latent – Uncorrectable

(*1) In case adjacent planes include a failing word line, it must be the word line for which the PSF event was reported.

(*2) "Detectable" -at least 1 failing WL is among the list of 8 physical word lines with middle page for TLC mode and 4 physical word lines for SLC mode defined as follows.
– TLC mode : WL 1, 7, 13, 32, 56, 79, 94, 111
– SLC mode : WL 0, 55, 56, 111

Table 12 Data Loss Classification for SLC 1P0V mode

Event	# of failing WLs		Classification
	Failing plane	Any adjacent plane	
ESF	-	-	ESF
Verify-UECC	Any	1	Time zero – Correctable
	Any other case		Time zero – Uncorrectable
Latent-UECC	1	0	Latent – Correctable
	Any other case		Latent – Uncorrectable

[Note] Kioxia S5E+BiCS5 MCP device does not allow to switch between SLC 1P0V and SLC 1P1V mode in the period from SOL to EOL.

2.4 Performance of Internal Raw NAND

Table 13 Performance of Internal Raw NAND (BiCS5 512Gb iTLC3)

Description	Operational Mode	Parameter	Value		Unit
			SLC mode	TLC mode	
Data Transfer Time from raw NDND cell to raw NAND register (typical case of page ave.)	Normal	tR	40	60	µs/page
	Fast tR		N/A	52	
	Longer tR		N/A	175(*2)	
Block Erase Time (the worst case of die ave. / timeout)	N/A	tBERS	15 / 30	15 / 30	ms
Program Time (the worst case of die ave.)	Normal	tPROG	60(*1)	330(*1)	µs/page
	Low Peak		65(*2)	360(*2)	
	SLC 1P1V		110(*1)	N/A	

(*1) “Tcase” range is from RT(25˚C) to 85˚C.

(*2) These value is based on measured data in raw NAND TCM.

2.5 Valid Blocks of Internal Raw NAND

Table 14 Valid Blocks of Internal raw NAND

KIOXIA's Part Number	Memory Die Type	Density	EOL	SOL	Unit
THGBY8G9A15LFAN	BiCS5 256Gb iTLC3	64GB	3,140	3,156	Blocks
THGBY8T0A25LFAN		128GB	6,280	6,312	Blocks
THGBY8T1A45LFAN		256GB	12,560	12,624	Blocks
THGBY8T2A85LFAN		512GB	25,120	25,248	Blocks
THGBY8T3AB5LFAP		1TB	50,240	50,496	Blocks

[Note] These values are the number of valid blocks in a package.
The number of valid blocks @SOL is guaranteed by Kioxia's outgoing test. However, the number of valid blocks @EOL cannot be guaranteed for all shipment Kioxia S5E+BiCS5 MCP devices, because Kioxia cannot perform EOL tests which could damage Kioxia S5E+BiCS5 MCP devices. Therefore, the specification of the number of valid blocks @EOL is evaluated by sampling and are guaranteed with average failure rate.
More than 70% of valid block per plane is guaranteed at Kioxia's outgoing test.

2.6 Boot Blocks of Internal raw NAND

Table 15 Boot Blocks of Internal raw NAND

Applicable Dies in Package	Blocks	Remark
Channel 0 – Die 0	Block#0 + 9blocks/Block#1~#15	Boot blocks are guaranteed by Kioxia's outgoing test.
Channel 0 – Die 1 Channel 1 – Die 0 Channel 1 – Die 1	3blocks/Block#0~#15	

[Note] Block number in this table is defined by the definition based on raw NAND block number.

2.7 00h Address ID of Internal Raw NAND die

Table 16 00h Address ID definition table of Internal Raw NAND

Cycle	Description	BiCS5 512Gb iTLC3	Comment
1st Data	Maker Code	98h	
2nd Data	Device Code	3Eh or 48h (*)	(*)3Eh: without CE sharing 48h: with CE sharing
3rd Data	Cell type, etc.	98h or 99h(*)	(*)98h: without CE sharing 99h: with CE sharing
4th Data	Page Size, etc.	03h	
5th Data	Plane Number, etc.	76h or 7Ah(*)	(*)76h: without CE sharing 7Ah: with CE sharing
6th Data	Technology Code	E4h	

2.8 Unique ID of Internal Raw NAND die

Table 17 Unique ID of Internal Raw NAND

Byte No.	Description	Value	Comment
0	Maker Code	01h	
1	Wafer Number (binary)	01h	Ex. Wafer = 1
2	Chip Location X (binary)	0Fh	Ex. X = 15
3	Chip Location Y (binary)	12h	Ex. Y = 18
4	9th digit of Lot Number (ASCII) – 20h	16h	Ex. CS0123456 36h, then 36h-20h=16h
5	8th digit of Lot Number (ASCII) – 20h	15h	Ex. CS0123456 35h, then 35h-20h=15h
6	1st digit of Lot Number (ASCII)	43h	Ex. CS0123456 43h
7	2nd digit of Lot Number (ASCII)	53h	Ex. CS0123456 53h
8	3rd digit of Lot Number (ASCII)	30h	Ex. CS0123456 30h
9	7th digit of Lot Number (ASCII) – 20h	14h	Ex. CS0123456 34h, then 34h-20h=14h
10	6th digit of Lot Number (ASCII) – 20h	13h	Ex. CS0123456 33h, then 33h-20h=13h
11	5th digit of Lot Number (ASCII) – 20h	12h	Ex. CS0123456 32h, then 32h-20h=12h
12	4th digit of Lot Number (ASCII) – 20h	11h	Ex. CS0123456 31h, then 31h-20h=11h
13-15	Vendor use	---	Vendor use area

3 Physical Interface

3.1 Block Diagram

Kioxia S5E+BiCS5 MCP device is equipped with 1 lane of PCIe interface. Additionally, only for Kioxia's internal test purpose, Kioxia S5E+BiCS5 MCP device is equipped with HW bypass interface, SPI, and JTAG interface. HW bypass interface is used to access internal Raw NAND. Figure 1 is a block diagram of Kioxia S5E+BiCS5 MCP device. Up to 16 raw NAND dies are connected to S5E controller.

External components (resisters and capacitance) shown in Figure 1 shall be followed because these are defined by S5E Controller Supplier. Please refer to "S5E Vendor Product Specification".

(*1) Kioxia S5E+BiCS5 MCP device does not support VPP function. VPP shall be connected to GND.
(*2) Kioxia S5E+BiCS5 MCP device uses internal VREF mode. Therefore, ANIx_VREF pins shall be opened.

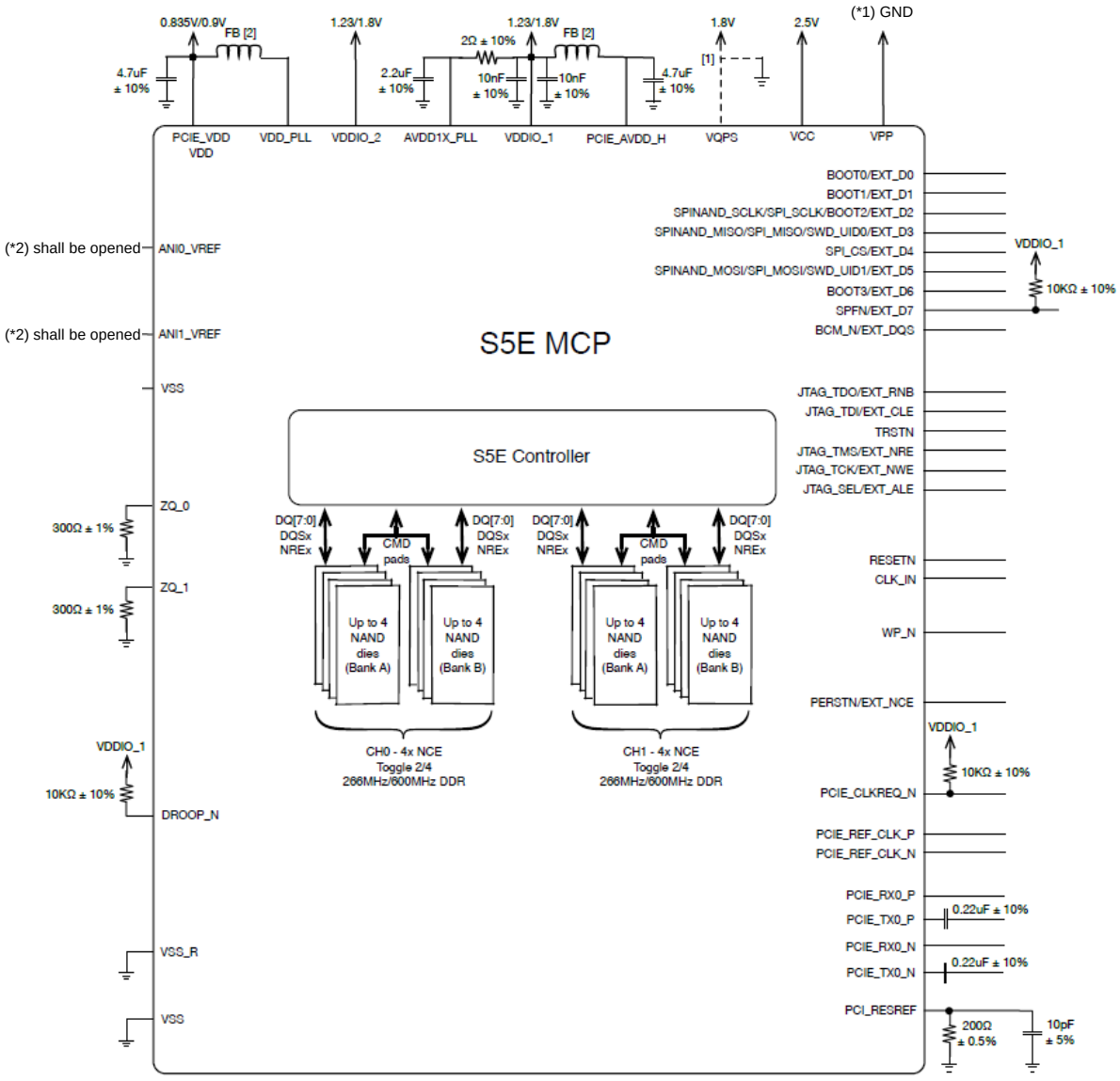

Figure 1 Physical Interface and Block diagram of Kioxia S5E+BiCS5 MCP device

3.2 Pin Assignment (Top View)

Figure 2 shows the pin assignment of Kioxia S5E+BiCS5 MCP device.

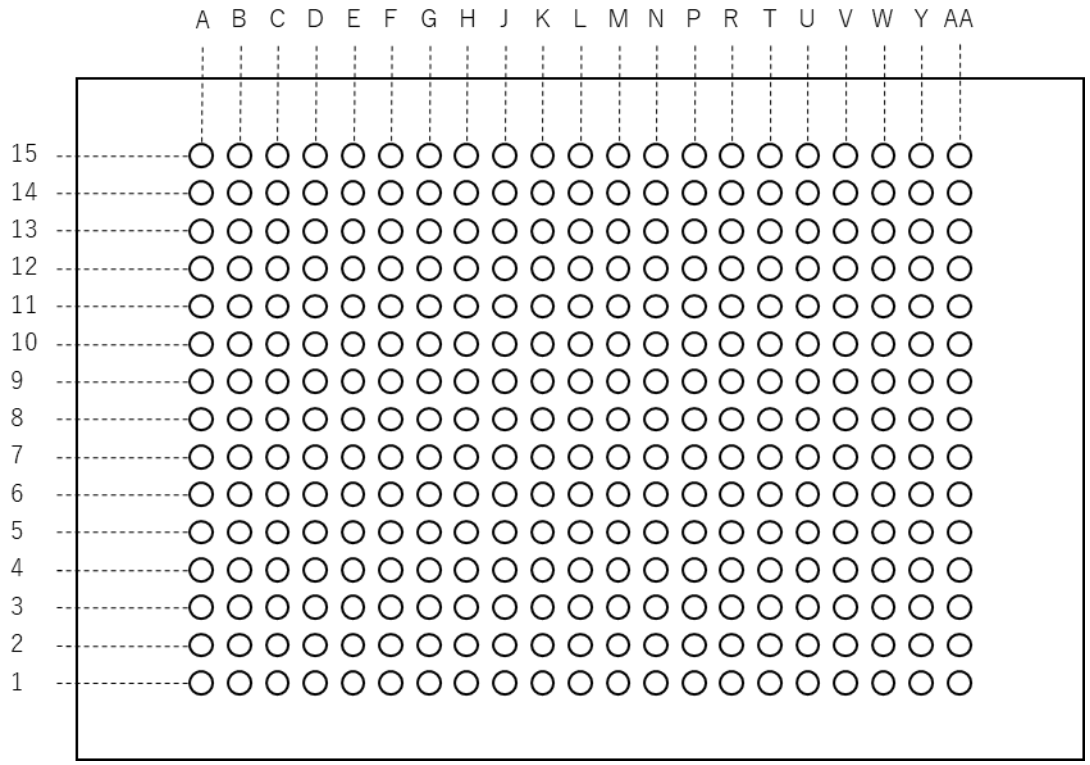

Figure 2 Pin Assignment (Top view)

3.3 Pin Names

Table 18 shows the pin location, name and description for Kioxia S5E+BiCS5 MCP device.

Table 18 Pin names and description

Pin Location	Signal Name	Type	Pad Type (*1)	Description
P9,P10	PCIE_AVDD_H	Power	-	PCIe 1.8V voltage supply
G5,G11,H5,H11,P5, P11,R5,R11	VDDIO_1	Power	-	External interface supply
G4,G12,H4,H12,K4, K12,L4,L12,M4,M12, P4,P12,R4,R12	VDDIO_2	Power	-	NAND IF IO Supply
N6	AVDD1X_PLL	Power	-	PLL voltage supply
H6	VQPS	Power	-	Fuse burning supply. VQPS should be connected to GND.
P7,R7,R9	PCIE_VDD	Power	-	PCIE digital supply
M6	VDD_PLL	Power	-	PLL digital supply
J7,J9,K7,K9,M7,M9, N7,N9	VDD	Power	-	Core digital supply
E11	VPP	Power	-	NAND supply S5E+BiCS5 MCP device doesn't support VPP function. VPP should be connected to GND.
E4,E12,F4,F12,T4,T12, U4,U12	VCC	Power	-	Power supply to the NAND array

Pin Location	Signal Name	Type	Pad Type (*1)	Description
A1,A2,A3,A4,A5,A6,A7, A8,A9,A10,A11,A12, A13,A14,A15,B1,B2, B3,B4,B5,B6,B7,B8,B9, B10,B11,B12,B13,B14, 15,C1,C2,C3,C4,C12, C13,C14,C15,D1,D2, D3,D13,D14,D15,E1, E2,E3,E13,E14,E15, F1,F2,F3,F5,F11,F13, F14,F15,G1,G2,G3, G13,G14,G15,H1,H2, H3,H7,H8,H13,H14, H15,J1,J2,J3,J4,J5, J8,J11,J12,J13,J14, J15,K1,K2,K3,K8,K13, K14,K15,L1,L2,L3,L7, L8,L9,L13,L14,L15, M1,M2,M3,M8,M13, M14,M15,N1,N2,N3, N5,N8,N12,N13,N14, N15,P1,P2,P3,P8,P13, P14,P15,R1,R2,R3, R6,R8,R10,R13,R14, R15,T1,T2,T3,T5,T7, T9,T11,T13,T14,T15, U1,U2,U3,U5,U7,U9, U11,U13,U14,U15,V1, V2,V3,V4,V5,V6,V7,V8, V9,V10,V11,V12,V13, V14,V15,W1,W2,W3, W4,W5,W6,W7,W8,W9, W10,W11,W12,W13, W14,W15,Y1,Y2,Y3,Y4, Y5,Y6,Y7,Y8,Y9,Y10, Y12,Y13,Y14,Y15,AA1, AA2,AA3,AA4,AA5, AA6,AA7,AA8,AA9, AA10,AA11,AA12, AA13,AA14,AA15	VSS	GND	-	Global chip ground
P6	PCIE_CLKREQ_N	I	1	PCIe clock request
U10	PCIE_TX0_P		2	Differential Tx lane 0
T10	PCIE_TX0_N		2	
U8	PCIE_RX0_P		2	Differential Rx lane 0
T8	PCIE_RX0_N		2	
T6	PCIE_REFCLK_P		2	Differential PCIe PHY reference clock
U6	PCIE_REFCLK_N		2	
N10	PCIE_RESREF		2	Reference pin. Requires 200Ω resistor in parallel to 10pF (*2).
N11	CLK_IN	I	1	24MHz Reference clock
J6	RESETN	I	1	Power on reset and Global reset

Pin Location	Signal Name	Type	Pad Type (*1)	Description
K11	ANI0_VREF	Reference Voltage	3	ANI0 voltage reference source. Output (Internal VREF) S5E+BiCS5 MCP device uses only internal VREF mode, and S5E Controller generates ANI0/ANI1 voltage references internally. Therefore, these pins shall be opened.
M5	ANI1_VREF	Reference Voltage	3	ANI1 voltage reference source. Output (Internal VREF) S5E+BiCS5 MCP device uses only internal VREF mode, and S5E Controller generates ANI0/ANI1 voltage references internally. Therefore, these pins shall be opened.
K5	ZQ_1	Calibration Pin	3	ANI1 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down (*2).
M11	ZQ_0	Calibration Pin	3	ANI0 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down (*2).
E5	WP_N	I	NA	Write protect. Connected to NAND
N4	DROOP_N		1	In functional mode, used as droop indication to SW.
G10	EXT_D7 / SPF_N	I/O	1 1.1 1.2	EXT_D7: Data for HW Bypass mode SPF_N: Sudden Power Fail notification
F9	EXT_D6 / BOOT3	I/O	1 1.1 1.2	EXT_D6: Data for HW Bypass mode Bootstrap3: Input enabled by default- for SW read.
E9	EXT_D5 / SPINAND_MOSI / SPI_MOSI / SWD_UID1	I/O	1 1.1 1.2	EXT_D5: Data for HW Bypass mode SPINAND_MOSI: SPI_MOSI in SPINAND mode SPI_MOSI: SPI_MOSI pin in SPI mode SWD_UID1: Proprietary GPIO Unique ID1
G9	EXT_D4 / SPI_CS	I/O	1 1.1 1.2	EXT_D4: Data for HW Bypass mode SPI_CS: SPI Chip Select
E8	EXT_D3 / SPINAND_MISO / SPI_MOSI / SWD_UID1	I/O	1 1.1 1.2	EXT_D3: Data for HW Bypass mode SPINAND_MOSI: SPI_MOSI in SPINAND mode SPI_MOSI: SPI_MOSI pin in SPI mode SWD_UID1: Proprietary GPIO Unique ID1
F8	EXT_D2 / BOOT2 / SPINAND_SCLK / SPI_SCLK	I/O	1 1.1 1.2	EXT_D2: Data for HW Bypass mode Bootstrap2: Input enabled by default for SW read SPINAND_SCLK: SPI_SCLK in SPINAND mode SPI_SCLK: SPI_SCLK pin in SPI mode

Pin Location	Signal Name	Type	Pad Type (*1)	Description
H9	EXT_D1 / BOOT1	I/O	1 1.1 1.2	EXT_D1: Data for HW Bypass mode Bootstrap1: Input enabled by default
G8	EXT_D0 / BOOT0	I/O	1 1.1 1.2	EXT_D0: Data for HW Bypass mode Bootstrap0: Input enabled by default
E10	EXT_DQS / BCM_N	I/O	1 1.3	EXT_DQS in HW_BYPASS (DDR) mode. BCM_N (Backward Compatibility Mode) bootstrap
F10	EXT_NCE / PERSTN	I	1	EXT_NCE: NCE for HW Bypass mode PERSTN: In functional mode, PCIe side reset event. SW handled.
G6	EXT_RNB / JTAG_TDO	O	1	EXT_RNB: RnB for HW Bypass mode JTAG_TDO: JTAG Test Data Output
E6	EXT_NRE / JTAG_TMS	I	1	EXT_NRE: NRE for HW Bypass mode JTAG_TMS: JTAG Test Mode Select
E7	EXT_ALE / JTAG_SEL	I	1	EXT_ALE: ALE for HW Bypass mode JTAG_SEL: JTAG Select
G7	EXT_CLE / JTAG_TDI	I	1	EXT_CLE: CLE for HW Bypass mode JTAG_TDI: JTAG Test Data In
F6	EXT_NWE / JTAG_TCK	I	1	EXT_NWE: NWE for HW Bypass mode JTAG Clock
F7	TRSTN	I	1	JTAG Test Reset
C5,C6,C7,C8,C9,C10, C11,D4,D5,D6,D7,D8, D9,D10,D11,D12,H10, J10,K6,K10,L5,L6,L10, L11,M10,Y11	NC	-	-	Non Connect (Floating individually)

(*1) Pad type 1 refers to all potential functional modes of the pad excluding bypass mode.
Pad type 1.1 refers to bypass mode SDR @1.23V.
Pad type 1.2 and 1.3 refer to bypass mode DDR @1.23V.

(*2) Electrical components specification for external connection shall be followed because these are defined by S5E Controller Supplier. Refer to “S5E Vendor Product Specification”.

4 DC Characteristics

4.1 IIH/IIL Pin Leakage Current specification

Table 19 ~ Table 24 show the IIL/IIH pin leakage current specification.

Table 19 IIH/IIL Pin Leakage Current Specification

Pin Name	Min [µA]	Max [µA]	Test Condition
			Input voltage [V]
EXT_NWE	-70.91 @1.8V -29.05 @1.23V	4	0 / 1.23 or 1.8
EXT_CLE			
EXT_NRE			
EXT_ALE	-4	63.21@1.8V 32.80@1.23V	
TRSTN			
EXT_DQS	-4	4	
EXT_NCE	-4	4	
EXT_RNB	-4	4	
EXT_D0	-4	4	
EXT_D1	-4	4	
EXT_D2	-4	4	
EXT_D3	-4	4	
EXT_D4	-4	4	
EXT_D5	-4	4	
EXT_D6	-4	4	
EXT_D7	-4	4	
PCIE_CLKREQ_N	-4	4	
RESETN	-4	4	
CLK_IN	-4	4	
DROOP_N	-4	4	
WP_N	-10	10	0 / 1.23

Table 20 IIH/IIL Pin Leakage Current Specification (ANI0_VREF pins)

Pin Name	Density [GB]	Min [µA]	Max [µA]	Test Condition Input voltage [V]
ANI0_VREF	S5E+BiCS5 512Gb iTLC3 MCP			
	64	-4.06	4.06	0 / 1.23
	128	-4.06	4.06	
	256	-4.13	4.13	
	512	-4.25	4.25	
	1024	-4.5	4.5	

Table 21 IIH/IIL Pin Leakage Current Specification (ANI1_VREF pins)

Pin Name	Density [GB]	Min [µA]	Max [µA]	Test Condition Input voltage [V]
ANI1_VREF	S5E+BiCS5 512Gb iTLC3 MCP			
	64	-4.00	4.00	0 / 1.23
	128	-4.06	4.06	
	256	-4.13	4.13	
	512	-4.25	4.25	
	1024	-4.5	4.5	

Table 22 IIH/IIL Pin Leakage Current Specification (ZQ_0 pins)

Pin Name	Density [GB]	Min [µA]	Max [µA]	Test Condition Input voltage [V]
ZQ_0	S5E+BiCS5 512Gb iTLC3 MCP			
	64	-1.63	1.63	0 / 1.23
	128	-1.63	1.63	
	256	-2.25	2.25	
	512	-3.5	3.5	
	1024	-6.0	6.0	

Table 23 IIH/IIL Pin Leakage Current Specification (ZQ_1 pins)

Pin Name	Density [GB]	Min [µA]	Max [µA]	Test Condition Input voltage [V]
ZQ_1	S5E+BiCS5 512Gb iTLC3 MCP			
	64	-1.00	1.00	0 / 1.23
	128	-1.63	1.63	
	256	-2.25	2.25	
	512	-3.5	3.5	
	1024	-6.0	6.0	

Table 24 IIH/IIL Pin Leakage Current Specification (PCIe IF pins)

Pin Names	Temperature [°C]	Min [µA]	Max [µA]	Test Condition Input voltage [V]
PCIE_REFCLK_P PCIE_REFCLK_N	-15	-10	10	0 / 0.835 or 0.9
PCIE_TX0_P PCIE_TX0_N		-5	5	
PCIE_RX0_P PCIE_RX0_N		-20	20	
PCIE_RESREF		-10	10	
PCIE_REFCLK_P PCIE_REFCLK_N	85	-20	20	
PCIE_TX0_P PCIE_TX0_N		-20	20	
PCIE_RX0_P PCIE_RX0_N		-40	40	
PCIE_RESREF		-20	20	

4.2 DC Characteristics except for IIH/IIL Pin Leakage

Table 25 shows DC characteristics for digital pins of Kioxia S5E MCP device except for IIH/IIL pin leakage.

Table 25 Other DC Characteristics except for IIH/IIL Pin Leakage

Parameter	Min	Typ	Max	Unit	Description
VIL	-0.3	-	0.3*VDDIO_1	V	Input low voltage
VIH @1.23V	0.7*VDDIO_1	-	1.3	V	Input high voltage @1.23V
VIH @1.8V	0.7*VDDIO_1	-	1.95	V	Input high voltage @ 1.8V
VOL	-	-	0.2*VDDIO_1	V	Output low voltage
VOH	0.8*VDDIO_1	-	-	V	Output high voltage
IOL @1.23V	2.4	4.6	7.5	mA	Low level output current @VOL(max). Pad type 1
IOH @1.23V	2.0	4.0	6.8	mA	High level output current @VOH(min). Pad type 1
IOL @1.8V	4.7	8.3	13.0	mA	Low level output current @VOL(max). Pad type 1
IOH @1.8V	4.9	8.9	14.2	mA	High level output current @VOH(min). Pad type 1
IOL @1.23V	8.0	14.9	24.0	mA	Low level output current @VOL(max). Pad type 1.1
IOH @1.23V	6.3	12.3	20.9	mA	High level output current @VOH(min). Pad type 1.1
IOL @1.8V	15.0	26.7	41.4	mA	Low level output current @VOL(max). Pad type 1.1
IOH @1.8V	15.0	27.0	43.2	mA	High level output current @VOH(min). Pad type 1.1
IOL @1.23V	5.0	9.4	15.2	mA	Low level output current @VOL(max). Pad type 1.2
IOH @1.23V	4.1	8.1	13.7	mA	High level output current @VOH(min). Pad type 1.2
IOL @1.8V	9.5	18.9	26.3	mA	Low level output current @VOL(max). Pad type 1.2
IOH @1.8V	10.0	18.0	28.7	mA	High level output current @VOH(min). Pad type 1.2
IOL @1.23V	3.5	6.5	10.5	mA	Low level output current @VOL(max). Pad type 1.3
IOH @1.23V	2.8	5.6	9.5	mA	High level output current @VOH(min). Pad type 1.3

Parameter	Min	Typ	Max	Unit	Description
IOL @1.8V	6.5	11.7	18.3	mA	Low level output current @VOL(max). Pad type 1.3
IOH @1.8V	6.9	12.5	20.0	mA	High level output current @VOH(min). Pad type 1.3
RPU @1.23V	49.1	79.5	148.3	kΩ	Pull up resistor @1.23V
RPD @1.23V	42.7	72.8	140.3	kΩ	Pull down resistor @1.23V
RPU @1.8V	26.9	40.3	68.8	kΩ	Pull up resistor @1.8V
RPD @1.8V	30.4	40.1	72.7	kΩ	Pull down resistor @1.8V
Cin	-	-	3	pF	Input capacitance (Controller's pad only)

[Note] These values are guaranteed by S5E Controller Supplier.

Pad types are defined in Table 18.

4.3 IDLE Power Current Specification

Table 26 IDLE Power Current Specification (Operation Mode 1)

Density [GB]	Temp [°C]	IDLE Clock Gated [mA]				IDLE Power Gated [mA]				IDLE Deep Power Gated [mA] (*1)			
		V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}	V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}	V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}
S5E+BiCS5 512Gb iTLC3 MCP													
64	85	65	2.5	0.95	0.15	18	0.4	0.2	0.15	18	0.58	0.2	0.15
	-15	11	1	0.95	0.15	1.6	0.2	0.2	0.15	1.6	0.38	0.2	0.15
128	85	65	2.5	0.95	0.26	18	0.4	0.2	0.26	18	0.58	0.2	0.26
	-15	11	1	0.95	0.26	1.6	0.2	0.2	0.26	1.6	0.38	0.2	0.26
256	85	65	2.5	0.97	0.36	18	0.4	0.22	0.36	18	0.58	0.22	0.36
	-15	11	1	0.97	0.36	1.6	0.2	0.22	0.36	1.6	0.38	0.22	0.36
512	85	65	2.5	0.97	0.48	18	0.4	0.22	0.48	18	0.58	0.22	0.48
	-15	11	1	0.97	0.48	1.6	0.2	0.22	0.48	1.6	0.38	0.22	0.48
1024	85	65	2.5	1.09	0.8	18	0.4	0.34	0.8	18	0.58	0.34	0.8
	-15	11	1	1.09	0.8	1.6	0.2	0.34	0.8	1.6	0.38	0.34	0.8

(*1) IDLE power current specification at "IDLE Deep Power Gated" state is measured in TCM.

Table 27 IDLE Power Current Specification (Operation Mode 2)

Density [GB]	Temp [°C]	IDLE Clock Gated [mA]				IDLE Power Gated [mA]				IDLE Deep Power Gated [mA] (*1)			
		V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}	V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}	V_{DD}	V_{CCQ} _IO	V_{CCQ} _ANI	V_{CC}
S5E+BiCS5 512Gb iTLC3 MCP													
64	85	60	1.2	0.95	0.15	16	0.4	0.2	0.15	16	0.52	0.2	0.15
	-15	10	0.6	0.95	0.15	1.5	0.2	0.2	0.15	1.5	0.32	0.2	0.15
128	85	60	1.2	0.95	0.26	16	0.4	0.2	0.26	16	0.52	0.2	0.26
	-15	10	0.6	0.95	0.26	1.5	0.2	0.2	0.26	1.5	0.32	0.2	0.26
256	85	60	1.2	0.97	0.36	16	0.4	0.22	0.36	16	0.52	0.22	0.36
	-15	10	0.6	0.97	0.36	1.5	0.2	0.22	0.36	1.5	0.32	0.22	0.36
512	85	60	1.2	0.97	0.48	16	0.4	0.22	0.48	16	0.52	0.22	0.48
	-15	10	0.6	0.97	0.48	1.5	0.2	0.22	0.48	1.5	0.32	0.22	0.48
1024	85	60	1.2	1.09	0.8	16	0.4	0.34	0.8	16	0.52	0.34	0.8
	-15	10	0.6	1.09	0.8	1.5	0.2	0.34	0.8	1.5	0.32	0.34	0.8

(*1) IDLE power current specification at “IDLE Deep Power Gated” state is measured in TCM.

5 AC Electrical Characteristics

This section describes AC electrical characteristics for each IO pad in the Kioxia S5E+BiCS5 MCP device. These specifications are guaranteed by S5E Controller Supplier

5.1 Digital Pins AC Characteristics (In HW Bypass Mode)

For AC characteristics of bypass mode pins, please refer to Chapter 3.1.3.4 in "S5E Vendor Product Specification".

5.2 Analog Pins AC Characteristics

Table 28 shows the AC characteristics of S5E+BiCS5 MCP device analog pins.

Table 28 AC Characteristics of S5E+BiCS5 MCP device for Analog Pins

Parameter	Min	Max	Unit	Description
t_up_WR_VREF @1.23V	-	4	µs	Ramp time of ANIx_VREF when VDDIO_2 = 1.23V
t_dis_WR_VREF	-	10	µs	Discharge time of ANIx_VREF with load in [*1]

[*1] Assuming load capacitance ≤65pF (S5E+BiCS5 MCP device, board, tester etc.)

5.3 JTAG IF AC Characteristics

Please refer to Chapter 2.7.3 in "S5E Vendor Product Specification".

5.4 SPI IF AC Characteristics

Please refer to Chapter 2.7.4 in "S5E Vendor Product Specification".

6 Power

6.1 Device Power Rails Partitioning

Table 29 Device Power Rails Partitioning

Symbol	Description	System rail
PCIE_AVDD_H	PCIe High voltage IO supply	VCCQ_IO
VDDIO_1	External interface GPIOs supply	VCCQ_IO
AVDD1x_PLL	PLL analog supply	VCCQ_IO
VDDIO_2	NAND IO	VCCQ_ANI
VQPS (*1)	Fuse burn supply	VQPS
VDD	Digital voltage domain for all Controller components	VDD
VDD_PLL	PLL voltage supply	VDD
PCIE_VDD	PCIe supply	VDD
VCC	NAND power supply	VCC
VPP (*2)	NAND power supply	VPP
VSS	Global chip ground	VSS

(*1) VQPS shall be tied to GND except for fuses burn.

(*2) Kioxia S5E+BiCS5 MCP device doesn't support VPP function.

6.2 Internal VREF Specification

For detailed description, please refer to Chapter 2.8.3 and 2.8.4 in "S5E Vendor Product Specification".

Table 30 Internal VREF Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VREFQ(DC)	Reference Voltage	--	0.49 x VCCQ_ANI	--	0.51 x VCCQ_ANI	V

[Note] S5E controller generates ANI0/ANI1 voltage references internally.

For testing purposes, VREF used by each of the controller IOs is output on VREF pins (One at a time). The expected DC level shall be (VccQ_ANI/2)/3 ± 20mV (VccQ_ANI = 1.23V).

6.3 Power Up Sequence

Figure 3 and Figure 4 show the power up sequence for Kioxia S5E+BiCS5 MCP device. Table 31 defines power up sequence timings.

*S5E+BiCS5 MCP device doesn't support VPP function.
Therefore, VPP pin shall be connected to GND.

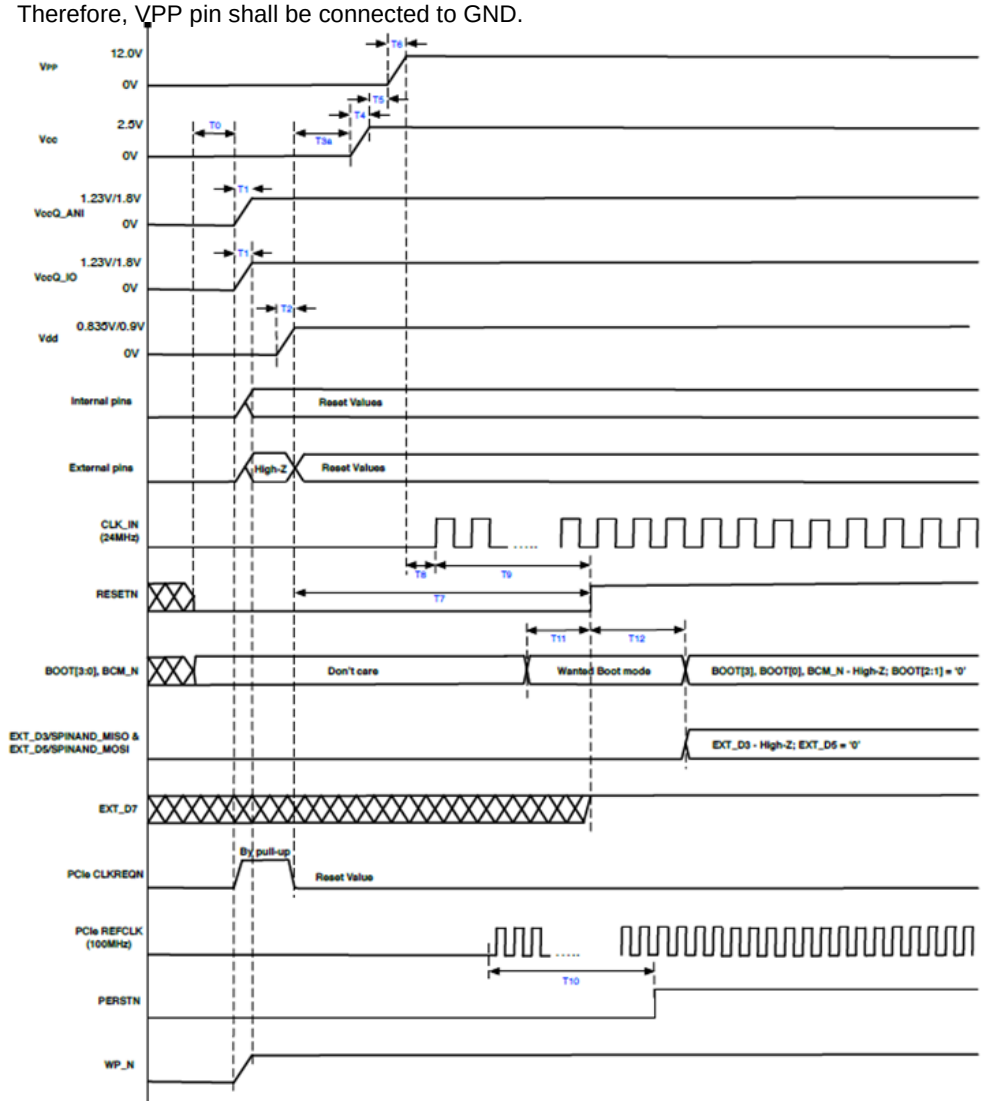

Figure 3 Power Up Sequence – VCCQ first

*S5E+BiCS5 MCP device doesn't support VPP function.
Therefore, VPP pin shall be connected to GND.

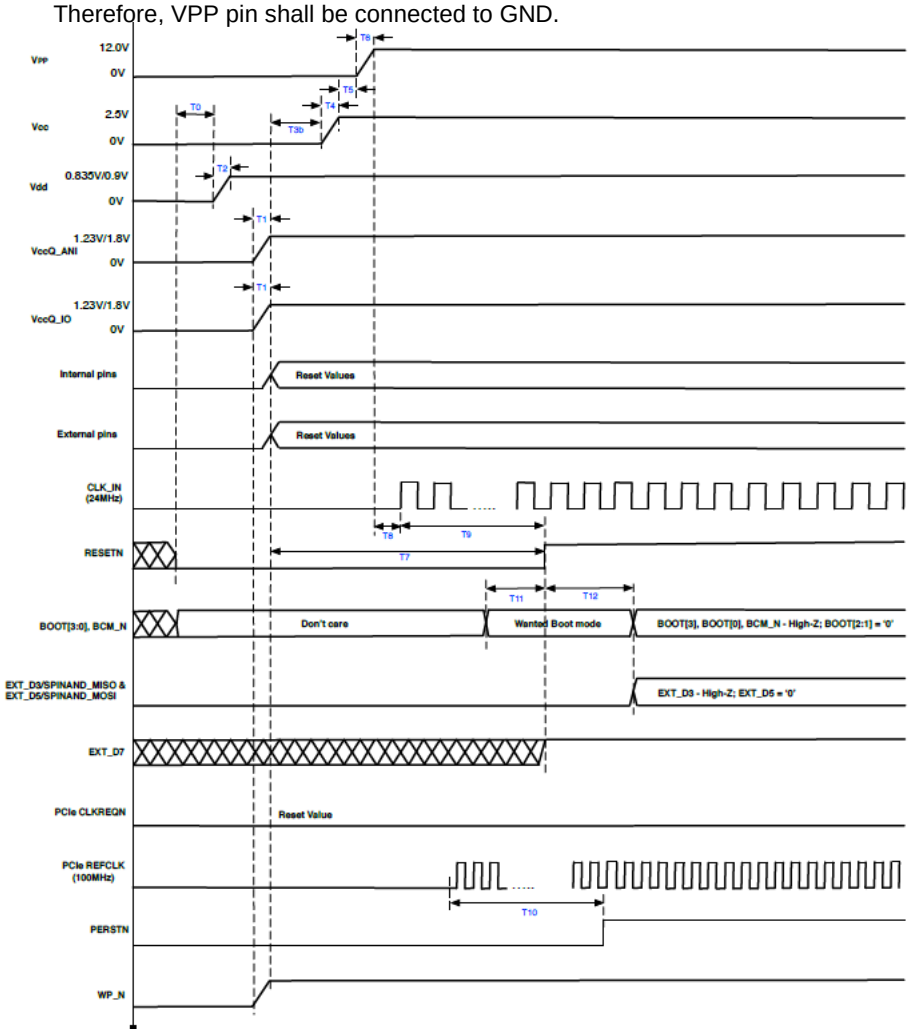

Figure 4 Power Up Sequence – VDD first

Table 31 Power Up Sequence Timing

Time	Description	Min	Max	Note
T0	Time from RESETN low till first Supply ramp start	0	-	(*)
T1	VccQ_ANI/IO supply ramp up	33.3 µs	4 ms	
T2	VDD supply ramp up time	16.7 µs	4 ms	(*)
T3a	Time from VDD supply ramp end till Vcc supply ramp start	0	-	(*)
T3b	Time from VccQ_ANI/IO supply ramp end till Vcc supply ramp start	0	-	(*)
T4	Vcc supply ramp up time	12.5µs	25 ms	
T5	Time from Vcc supply ramp end till VPP supply ramp start	0	-	(*)
T6	VPP supply ramp up time	TBD	TBD	(*)
T7	Time from VDD & VccQ_ANI/IO supplies are up till RESETN de-assertion	100 µs	-	(*)
T8	Time from VPP till CLK_IN starts toggling	0	-	(*)
T9	Time CLK_IN to be active before RESETN de-assertion	32 CLK_IN	-	(*)

Time	Description	Min	Max	Note
T10	Time from PCIe REFCLK starts toggling until PERSTN de-assertion	100 µs	-	(*)
T11	Time BOOT[3:0], BCM_N & MISO/MOSI have to be stable before RESETN de-assertion	0	-	(*)
T12	Time from RESETN de-assertion till BOOT[3:2,0], BCM_N, MISO/MOSI can be floated	5 ms	-	(*)

(*) These values are guaranteed by S5E Controller Supplier.

6.4 Power Down Sequence

Figure 5 and Figure 6 shows the power down sequence for KIOXIA S5E MCP device. Power down sequence shall be initiated only when there are no pending commands.

*S5E+BiCS5 MCP device doesn't support VPP function.
Therefore, VPP pin shall be connected to GND.

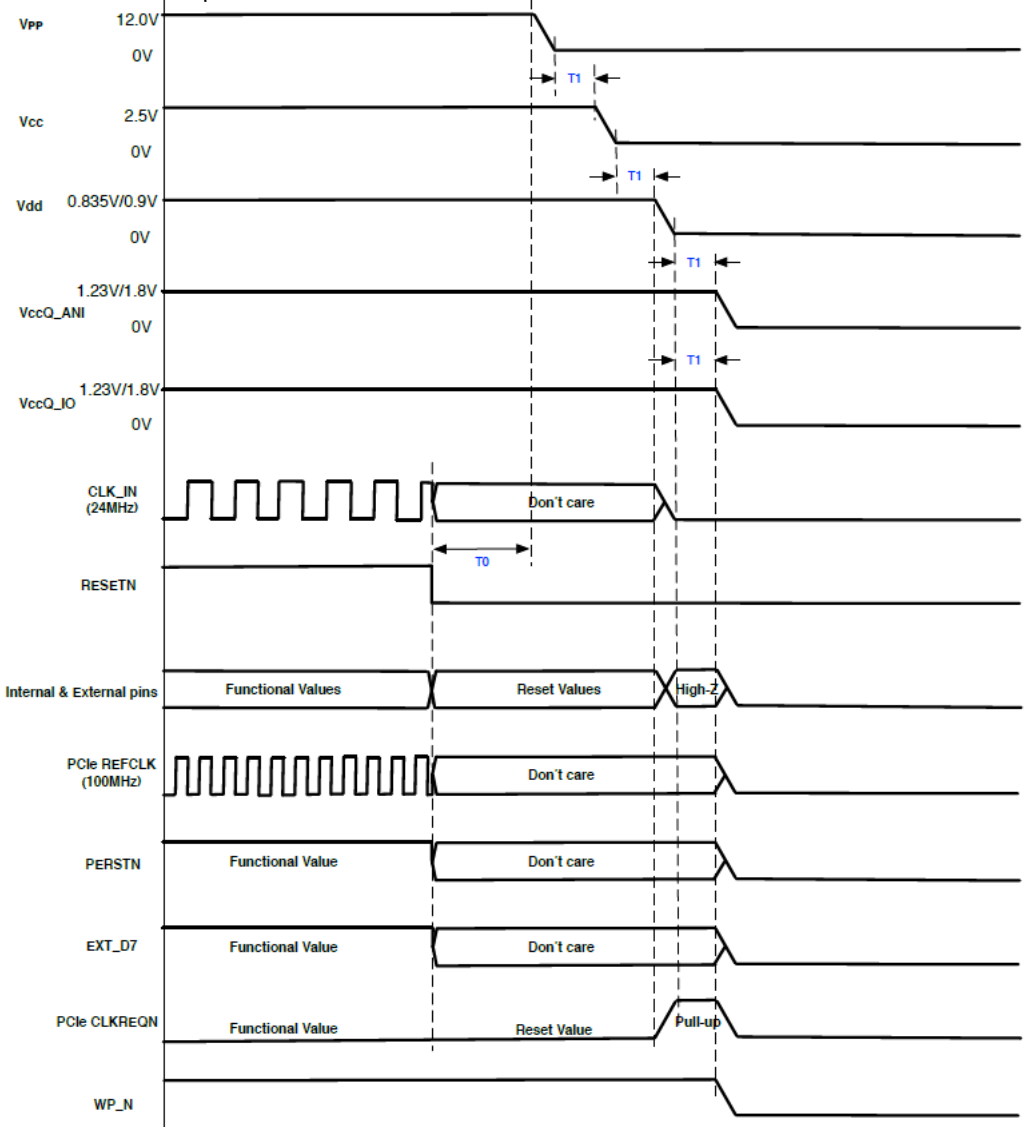

Figure 5 Power Down Sequence– VDD first

*S5E+BiCS5 MCP device doesn't support VPP function.
Therefore, VPP pin shall be connected to GND

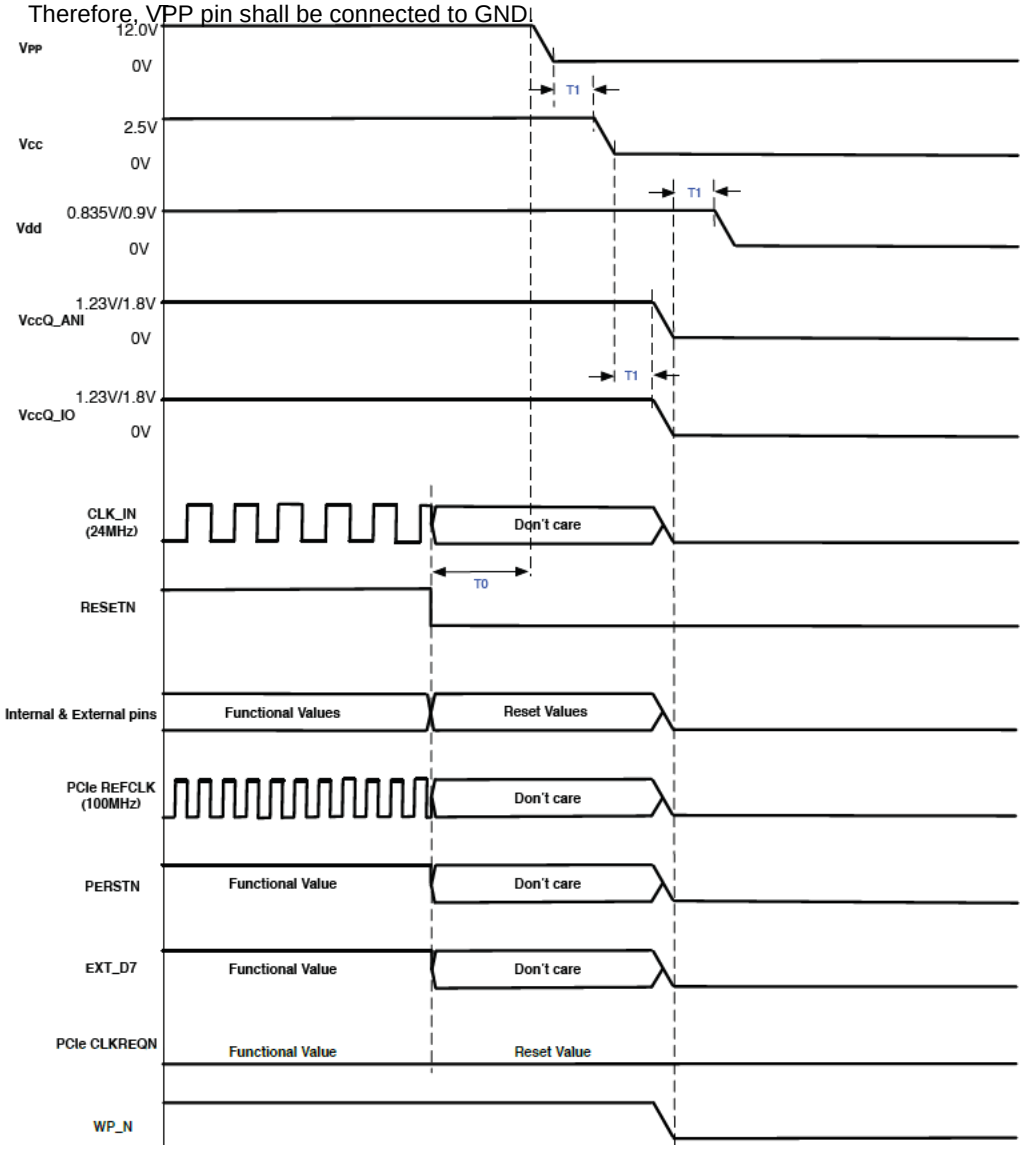

Figure 6 Power Down Sequence– VCCQ first

Table 32 Power Down Sequence Timing

Time	Description	Min	Max
T0	Time from RESETN assertion till VPP Supply ramp down start	TBD	-
T1	Time from any supply down (0V) till next supply starts powering down	0	-

[Note] This value is guaranteed by S5E Controller Supplier.

6.5 RESETN Sequence

Figure 7 shows the RESETN sequence. RESETN sequence initializes entire S5E+BiCS5 MCP device same as power on reset, and shall be initiated only when there are no pending commands.

*S5E+BiCS5 MCP device doesn't support VPP function.
Therefore, VPP pin shall be connected to GND.

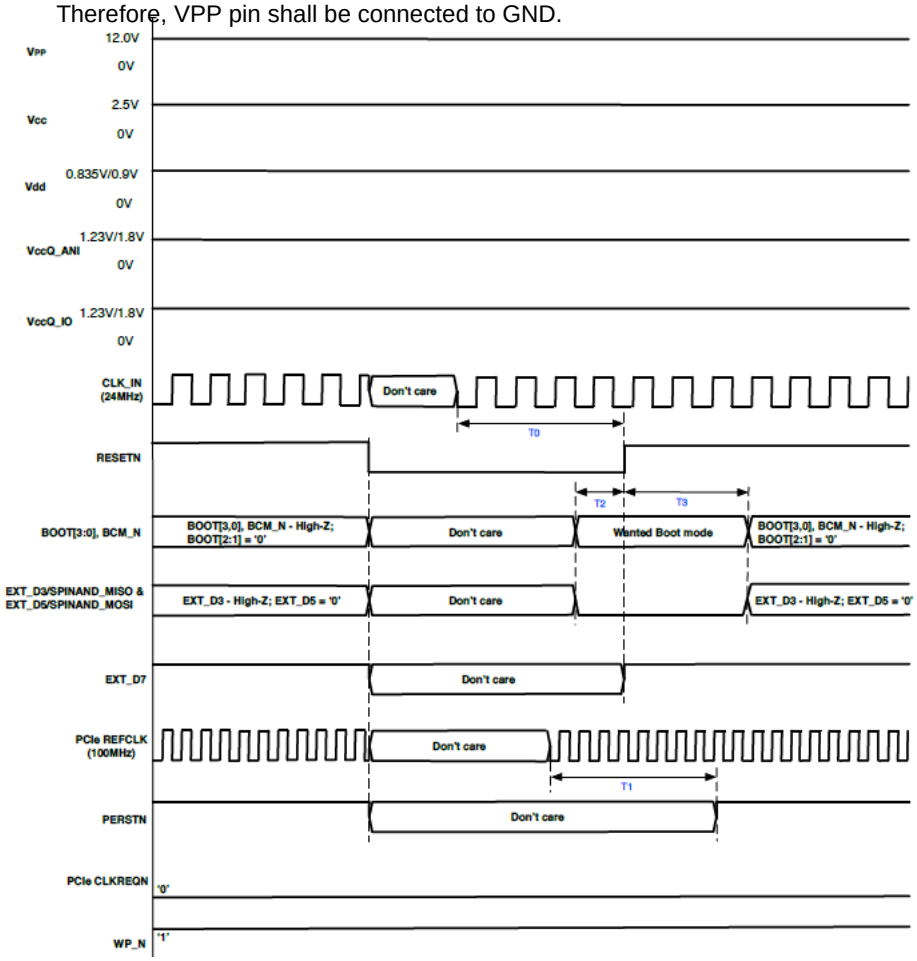

Figure 7 RESETN Sequence

Table 33 RESETN Sequence Timing

Time	Description	Min	Max
T0	Time CLK_IN should toggle before RESETN may be de-asserted	100 µs	-
T1	Time from REFCLK starts toggling till PERSTN can de-assert	100 µs	-
T2	Time BOOT[3:0] & BCM_N have to be stable before RESETN de-assertion	0	-
T3	Time from RESETN de-assertion till BOOT[3:2,0] BCM_N, MISO/MOSI can be floated [1]	5 ms	-

[Note] This value is guaranteed by S5E Controller Supplier.

6.6 Boot Up Power Mode

Kioxia S5E+BiCS5 MCP device has the following boot modes:

1. Low Power – S5E+BiCS5 MCP device boots to reduced frequencies using 24MHz CLK_IN and 100MHz PCIE_REFCLK. ANI is starting at 12MHz DDR and switching during the boot to 33MHz DDR.
2. Normal – S5E+BiCS5 MCP device boots to nominal frequencies using 24MHz CLK_IN and 100MHz PCIE_REFCLK. ANI is starting at 12MHz DDR and switching during the boot to 266MHz/600MHz DDR.
3. Boot From Host (BFH) – S5E+BiCS5 MCP device boots from PCIe host. Boot ends in Low Power mode.
4. Test Mode 1 – S5E Controller in Idle
5. Pads Test Mode – Enables external pads leakage measurement (Without FW need)
6. HW Bypass – SDR mode 1.23V – Enables direct access to internal raw NAND in SDR while ANI is working @1.23V (VccQ_ANI)
7. HW Bypass – DDR mode 1.23V – Enables direct access to internal raw NAND in DDR while ANI is working @1.23V (VccQ_ANI)

Table 34 Boot Mode Selection

BOOT[3]	BOOT[2]	BOOT[1]	BOOT[0]	Boot Mode
X	0	0	0	Low power boot
X	0	0	1	Normal boot
X	0	1	X	Boot from Host
0	1	0	1	Test Mode 1
0	1	1	0	Pads test mode
1	1	1	1	HW bypass – SDR mode 1.23V
1	1	0	1	HW bypass – DDR mode 1.23V

[Note] Boot mode transition and its transition time is measured in TCM.

6.7 Power Modes

S5E+BiCS5 MCP device has the following power modes:

Table 35 Power Modes

Power Mode	Internal frequencies	ANI frequency	PCIe Link state	Controller's login state
OFF	N/A	N/A	N/A	N/A
Reset	N/A	N/A	Reset	Reset
LP Mode	Low	33MHz DDR	Gen1 + L1.ss (*1)	Active
Normal Mode	High	266MHz/600MHz DDR	Gen3/4 + L1.ss (*1)	Active
Boot From Host	Low	33MHz DDR	Gen1 + L1.ss (*1)	Active
Clock Gated	N/A	N/A	L1.2	Clock Gated
Power Gated	N/A	N/A	L1.2	Power Gated
Deep Power Gated	N/A	N/A	L2/L3	Power Gated
HW Bypass	N/A	(*2)	N/A	Power Gated
Pads Test Mode	N/A	N/A	N/A	Power Gated
Test Mode 1	N/A	N/A	N/A	Idle

(*1) Host is responsible to limit PCIe link to Gen1.

(*2) Please refer to Chapter 3.1 in "S5E Vendor Product Specification".

[Note] Power mode transition and its transition time is measured in TCM

[Note] If host supports L1 only (without its sub-states) S5E+BiCS5 MCP device will not be able to enter Clock/Power Gated modes. S5E+BiCS5 MCP device will remain in the same power mode it was in and PCIe link will go to L1.

[Note] L1.ss, L1.2, L2, and L3 are defined as link power state levels of PCIe. Please refer to "S5E Controller Datasheet".

6.8 Power Mode Transition Flow

Figure 8 shows boot flow and transition between various power states.

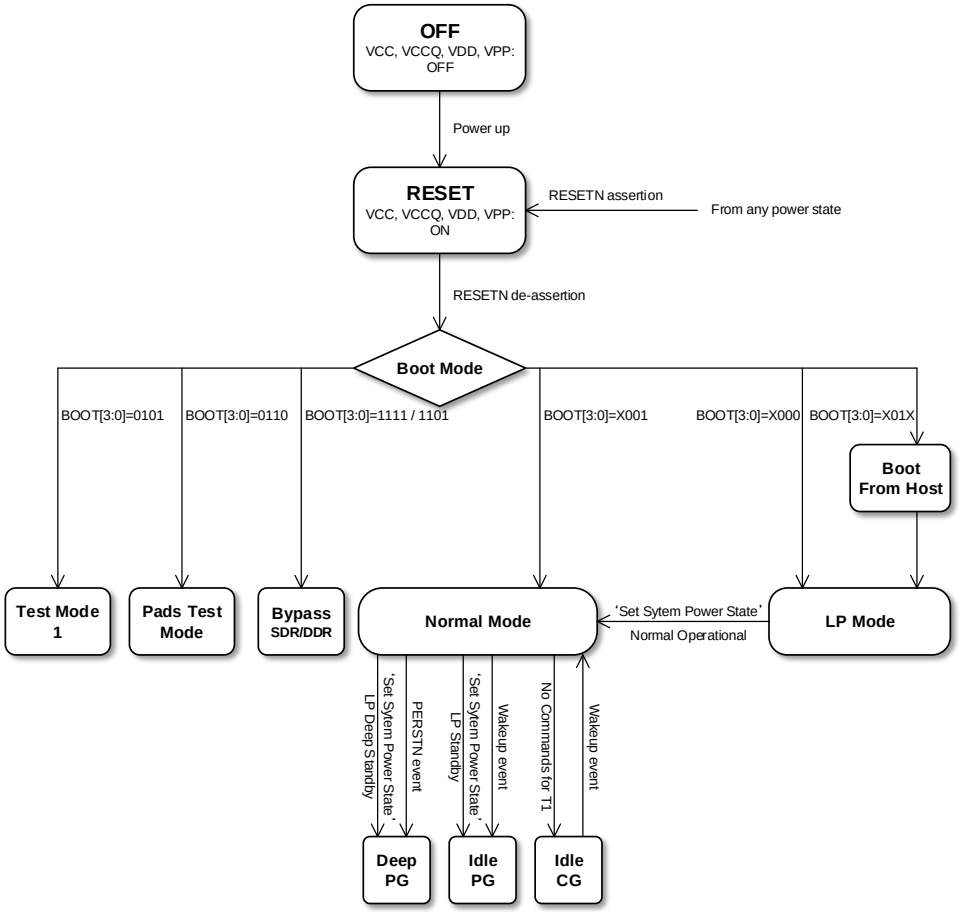

Figure 8 Power Mode Transition Diagram

Table 36 Target Transition time for Power Mode

Beginning State	Target State	Max
Off	LP mode	TBD
Off	Normal mode	TBD
LP mode	Normal mode	(*1)
Normal mode	Idle CG	TBD
Normal mode	Idle PG	TBD
Normal mode	Deep PG	TBD
Idle Clock Gated (CG)	Normal mode	(*1)
Idle Power Gated (PG)	Normal mode	(*1)
Deep PG	Normal mode	(*2)

(*1) Power mode transition and its transition time is measured in TCM. Please refer to Table 37 and Table 38.

(*2) Deep PG → Normal latency is mainly dependent on PCIe host enumeration time.

Table 37 Target Transition time for Power Mode in Operation Mode 1 (Measured in TCM)

Density [GB]	LP → Normal	CG → Normal	PG → Normal	Unit
S5E+BiCS5 512Gb iTLC3 MCP				
64	1433.6	43.8	294.8	µs
128	1903.4	44.1	308.1	µs
256	2833.7	45.3	320.3	µs
512	4671.5	44.4	343.4	µs
1024	8306.9 (*)	45.3	388.3	µs

(*) The target value is 8ms for 1024GB. A waiver was granted by Apple

Table 38 Target Transition time for Power Mode in Operation Mode 2 (Measured in TCM)

Density [GB]	LP → Normal	CG → Normal	PG → Normal	Unit
S5E+BiCS5 512Gb iTLC3 MCP				
64	1438.6	45.4	293.4	µs
128	2582.0	59.1	468.1	µs
256	4001.9	59.2	485.2	µs
512	6846.3	59.5	513.5	µs
1024	12436.3	59.2	572.2	µs

7 Operational FW features

The operation of the FW is guaranteed by S5E Controller Supplier. As for Register & Command definitions, please refer to "ASI Specification" document.

7.1 Device Parameter Table

Table 39 Device Parameter Table

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Parameter Page Header	0	16	"ASI Device Info"	Header "ASI Device Info", Padded with zero
Protocol Revision	16	3	"1.5.19"	Defines the revision of ASI protocol in the following format – <Major>.<Minor>.<Revision>.
Padding	19	1	0	Padded with zeroes
Interface Revision	20	4	130	Vendor specific designator for Interface revision. If not used, returns zeroes
SWD ID	24	1	0	2-bit chip ID, padded with zeroes to byte. The default is set by the bootstrap I/O
Padding	25	3	0	Padded with zeroes
Max Num Commands	28	2	447	2 bytes describing the maximum number of commands that can be handled by the controller simultaneously. Same as the MAX_NUM_COMMANDS register on the bar
Reserved	30	1	0	Padded with zeroes
MAX_DEBUG_ BUFFERS	31	1	1	1 byte describing maximum number of the debug buffers.
Channels/Package	32	1	1DP: 1, 2DP: 2, 4DP: 2, 8DP: 2, 16DP: 2	1 byte describing the number of channels per package
Maximum Chip Enable/Channel	33	1	1DP: 1, 2DP: 1, 4DP: 2, 8DP: 4, 16DP: 4	1 byte describing the number of chip enable signals per channel.
Maximum Dies/Channel	34	1	1DP: 1, 2DP: 1, 4DP: 2, 8DP: 4, 16DP: 8	1 byte describing the number of dies per channel.
Planes/Die	35	1	2	1 byte describing the number of planes in die
Blocks/Plane	36	2	512Gb: 1662,	2 bytes describing the number of blocks/plane

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Word lines/Block	38	2	448	2 bytes describing the number of word lines/block
SLC pages per block	40	2	448	2 bytes describing the number of SLC pages per block
MLC/TLC/QLC pages per block	42	2	1344	2 bytes describing the number of MLC/TLC pages per block
Bytes/Single Plane Page	44	2	18336	2 bytes describing the number of bytes per single plane page
Sectors/Plane in Normal Mode	46	1	4	Number of sectors (Data + Metadata) in a single plane in normal mode.
Sectors/Plane in Raw Mode	47	1	5	Number of sectors (Data + Metadata) in a single plane in raw mode.
Sectors/Plane in Normal Mode for joint programming	48	1	12	Number of sectors (Data + Metadata) in a single plane in normal mode for joint programming (all page types are accessed together).
Sectors/Plane in Raw Mode for joint programming	49	1	15	Number of sectors (Data + Metadata) in a single plane in raw mode for joint programming (all page types are accessed together).
Bits/Cell	50	1	5	1 byte describing the supported bits/cell using a bitmap Bit 0 – 1bit/cell Bit 1 – 2bit/cell Bit 2 – 3bit/cell Bit 3 – 4bit/cell Bit 7-4 – Reserved
Padding	51	1	0	Padded with zeroes
Die Density	52	2	512Gb: 512	Total number of Gbits per die
Guaranteed Good Blocks/Plane (*1)	54	2	512Gb: 1570	Guaranteed number of good blocks per die (package average) throughout the device life
Max interface speed	56	2	Operation Mode 1: 266 Operation Mode 2: 600	Maximum interface speed supported by the device in MHz
Min interface speed	58	2	Operation Mode 1: 200 Operation Mode 2: 480	Minimum interface speed supported by the device in MHz in Normal Mode

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
SOL Guaranteed Good Blocks/Die (*1)	60	2	512Gb: 3156	Guaranteed number of good blocks/die at the start the device life
Guaranteed Good Blocks/Die (*1)	62	2	512Gb: 3140	Guaranteed number of good blocks/die throughout the device life
NAND Vendor ID	64	1	5	NAND Vendor Id – 0x05 - KIOXIA
NAND Lithography	65	1	4	NAND Lithography – For BiCS FLASH NANDs -
NAND Technology	66	1	1	Planar NAND – 0 BiCS FLASH NAND – 1 0x2-0xFF - reserved
NAND Revision	67	1	0	Revision of the die
Data Format Revision	68	1	1	Revision of the data format written to the NAND. It is required to completely erase the device if the Data Format revision is changed since it may be undecodable.
Padding	69	3	0	Padded with zeroes
FW Version	72	64	"s5e.ofw.toshiba_tlc_3d_g5_2p_512gb-3.11.0.0.22.0" 8DP: "s5e.ofw.toshiba_tlc_3d_g5_2p_512gb-3.11.0.1.3.0"	Get version of current FW running on the device. All 00h or all FFh indicates invalid FW
Production FW Version	136	64	"3.11.0.0.22.0" 8DP: "3.11.0.1.3.0"	Returns an ID of the FW used during the production of the device. If unused, returns zeroes.
Package Assembly Code	200	16	0	Not used – returns zeroes.
Controller Unique ID	216	16	Depend on each devices	Unique identifier of the controller die
Controller HW ID	232	16	"A1"	Controller version described as an alpha-numeric string
NAND die unique ID	248	256	Depend on each devices	16 bytes for each die unique ID. Unused dies shall be marked with 0xFF
NAND die Chip ID	504	8	0x00, 0x00, 0x98, 0x3E, 0x98, 0x03, 0x76, 0xE4 (Only 16DP): 0x00, 0x00, 0x98, 0x48, 0x99, 0x03, 0x7A, 0xE4	NAND die chip ID

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Reserved	512	16	0	Padded with zeroes
System Mode 3 Exit Latency	528	4	1000	System Mode 3 Exit latency
Max Program/Read Buffers	532	1	1	Maximum number of buffers that can be used in Program/Read to/from RAM commands.
Padding	533	3	0	Padded with zeroes
FW Size	536	8	0	FW Size in bytes
Command Support Bitmap	544	32	0xFB 0x0F 0xF3 0x00 0x0F 0x00 0x7F 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0xE2 0xFF 0xFF 0x01 0xDA 0x1D 0x3C 0x00 0x00 0x00 0x00 0x00 0x00	Bitmap vector of 256 entries that defines which commands are supported. Byte 0, bit 0 defines support of command type 0x00 Byte 1, bit 0 defines support of command type 0x08 ... Byte 7, bit 7 defines support of command type 0xff Value of 1 indicates that the command is supported.
Programming Order Table Size Type=Native	576	2	3584	Number of programming order table size
NAND Physical Structure Table Size	578	2	5384	Number of NAND physical structure table size
Native Read-Verify Commands/Block	580	2	448	Number of times that the host shall call Read-Verify command after TLC programming
Failing Dies Bitmap	582	2	0	Bitmap indicating dies failure as detected by the controller – Bit0 – channel 0, die 0 – 0 = Die active, 1 = Die failure Bit7- channel 0, die 7 – 0 = Die active, 1 = Die failure Bit8 – channel 1, die 0 – 0 = Die active, 1 = Die failure Bit15- channel 1, die 7- 0 = Die active, 1 = Die failure

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Device Context Size	584	4	16384	Number of bytes in Device Context. The host shall read this parameter before Set/Get Device context to obtain the command SIZE field
Maximum None SLC Guaranteed Grown Bad Blocks/Die (*1)	588	2	512Gb: 16	Maximum number of guaranteed grown bad blocks per die when the device is programmed in none-SLC mode
Die Density fraction	590	2	0	The fraction of the die density, specified in Mbit in case of non-integer size in Gbit (as specified in Die Density) field.
Configuration Vector Validity	592	1	1	0 – Not Valid 1 – Valid
Padding	593	3	0	
Configuration Vector	596	8	512Gb-1DP: 0x1B 0xA1 0x00 0x08 0x01 0x00 0x00 0x00 512Gb-2DP: 0x1B 0xA1 0x00 0x88 0x01 0x00 0x00 0x00 512Gb-4DP: 0x1B 0xA1 0x00 0x88 0x51 0x00 0x00 0x00 512Gb-8DP: 0x1B 0xA1 0x00 0x88 0xF1 0x00 0x00 0x00 512Gb-16DP: 0x1B 0xA1 0x00 0x88 0xF1 0x01 0x00 0x00	Binary value
Reserved	604	2	0	
SLC Pages per Boot Block	606	2	448	Number of SLC pages per boot block
Native Reduced Read Verify Commands Per Block	608	2	32	Number of times that the host shall call Read-Verify command after Native mode programming (reduced mode)
SLC Read Verify Commands Per Block	610	2	448	Number of times that the host shall call Read-Verify command after SLC programming
SLC Reduced Read Verify Commands Per Block	612	2	16	Number of times that the host shall call Read-Verify command after SLC programming (reduced mode)

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Number of Dies per Channel 0	614	1	1DP:1, 2DP: 1, 4DP: 2, 8DP: 4, 16DP: 8	Offset [0] – Number of dies in Channel 0 Offset [1] – Number of dies in Channel 1 "Maximum Dies per Channel" field is defined using these parameters. For instance, if number of dies in channel zero is four and in channel one is eight, value of this parameter is eight. Valid values are 0 to 8
Number of Dies per Channel 1	615	1	1DP: 0, 2DP: 1, 4DP: 2, 8DP: 4, 16DP: 8	
NAND VCCQ Voltage	616	1	1	0 – VCCQ is 1.8v 1 – VCCQ is 1.2v
CE Mapping	617	8	1DP: 0x01 0x00 0x00 0x00 0x00 0x00 0x00 0x00 2DP: 0x01 0x00 0x00 0x00 0x01 0x00 0x00 0x00 4DP: 0x01 0x01 0x00 0x00 0x01 0x01 0x00 0x00 8DP: 0x01 0x01 0x01 0x01 0x01 0x01 0x01 0x01 16DP: 0x02 0x02 0x02 0x02 0x02 0x02 0x02 0x02	Mapping of controller chip enable signals to NAND. "Maximum Chip Enable / Channel" field is defined as the maximum of these eight parameters
Strings per WL	625	1	4	Number of strings per WL
Allowed keeping SLC blocks in erased state	626	1	1	0x0 – Not Allowed 0x1 – Allowed 0x2-0xFF - Reserved
MCP-ID	627	40	Depend on each devices	Reserved for future use
Programming Order Table Size Type=SLC	667	2	3584	Number of programming order table size for SLC.
Programming Order Table Size Type=Protected SLC	669	2	3584	Number of programming order table size for Protected SLC.
Programming Order Table Size Type=Reserved1	671	2	0	Reserved
Programming Order Table Size Type=Reserved2	673	2	0	Reserved
Programming Order Table Size Type=Reserved3	675	2	0	Reserved
Block Scan - Number of pages in Native mode	677	2	1344	Number of Multi-Plane pages per block to read for Block Scan in Native mode

Field Name	Offset [Bytes]	Size [Bytes]	Value	Notes
Block Scan - Number of pages in SLC mode	679	2	448	Number of MP pages per block to read for Block Scan in SLC mode
NAND Maturity	681	1	Depend on each devices	Trim identifier. 0x0 – Early (WS, ES, etc.) 0x1 – CS candidate 0x2 – CS (if trim changes) 0x3..F – Reserved for late trim changes Other Values – Reserved
NAND Functionality Revision	682	1	0	0x0 – Baseline functionality 0x1..F – Functional change #1, #2,.. Other Values – Reserved
Cross-MSP Coherency ID	683	4	Depend on each devices	An ID uniquely describing a set of coherency parameters. This value should be used to verify coherency across connected MSPs.
Block scan data size in sectors	687	1	3	Block scan data size in sectors for Block Scan Pause/Resume commands
Package Type	688	1	Only 16DP :1 2	Package form factor: 0 = Standard 1 = Mini 2 = Micro

(*1) These parameters are used by Apple's host for Apple internal purposes. Guaranteed good blocks spec of internal BiCS5 is described in Table 14 and Table 15 .

8 Package Dimensions (Rev.1.0)

1. P-VFLGA315-0914-0.50-002 (Micro Package 0.87mm Z-max)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

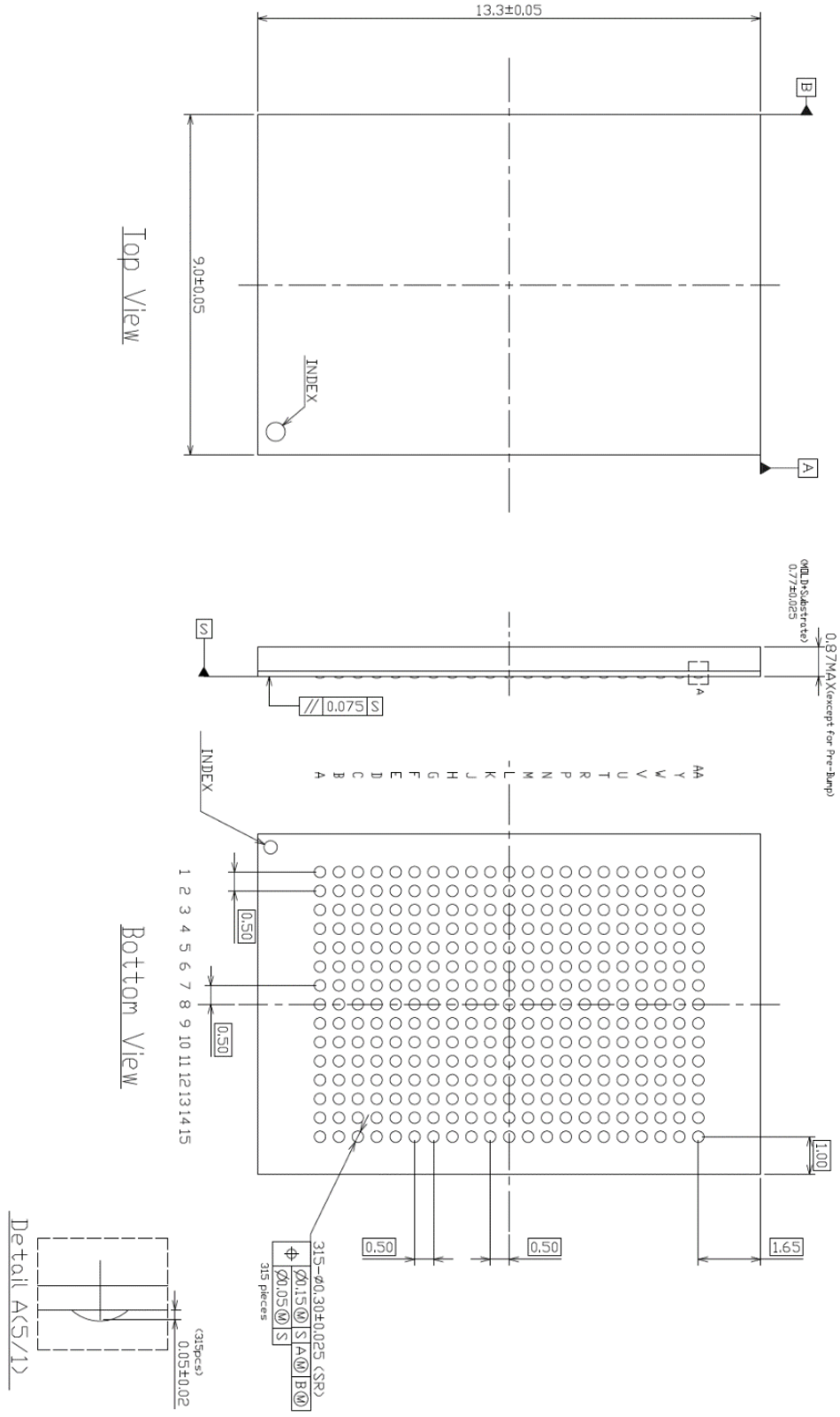

Figure 9 Package Dimension of P-VFLGA315-0914-0.50-002

2. P-VFLGA315-0914-0.50-001 (Micro Package 0.9mm Z-max)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

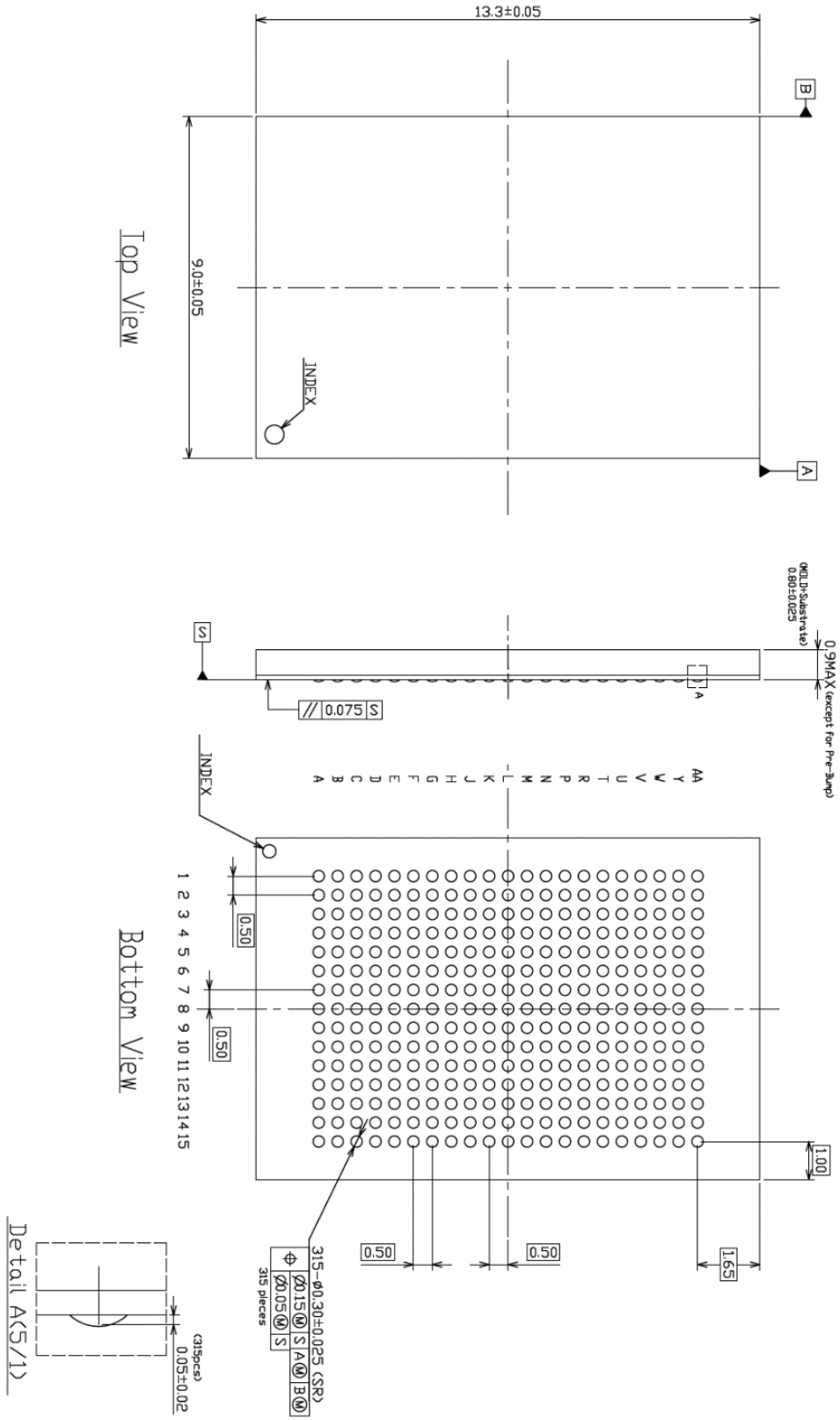

Figure 10 Package Dimension of P-VFLGA315-0914-0.50-001

3. P-FLGA315-1114-0.50-001 (Mini Package)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

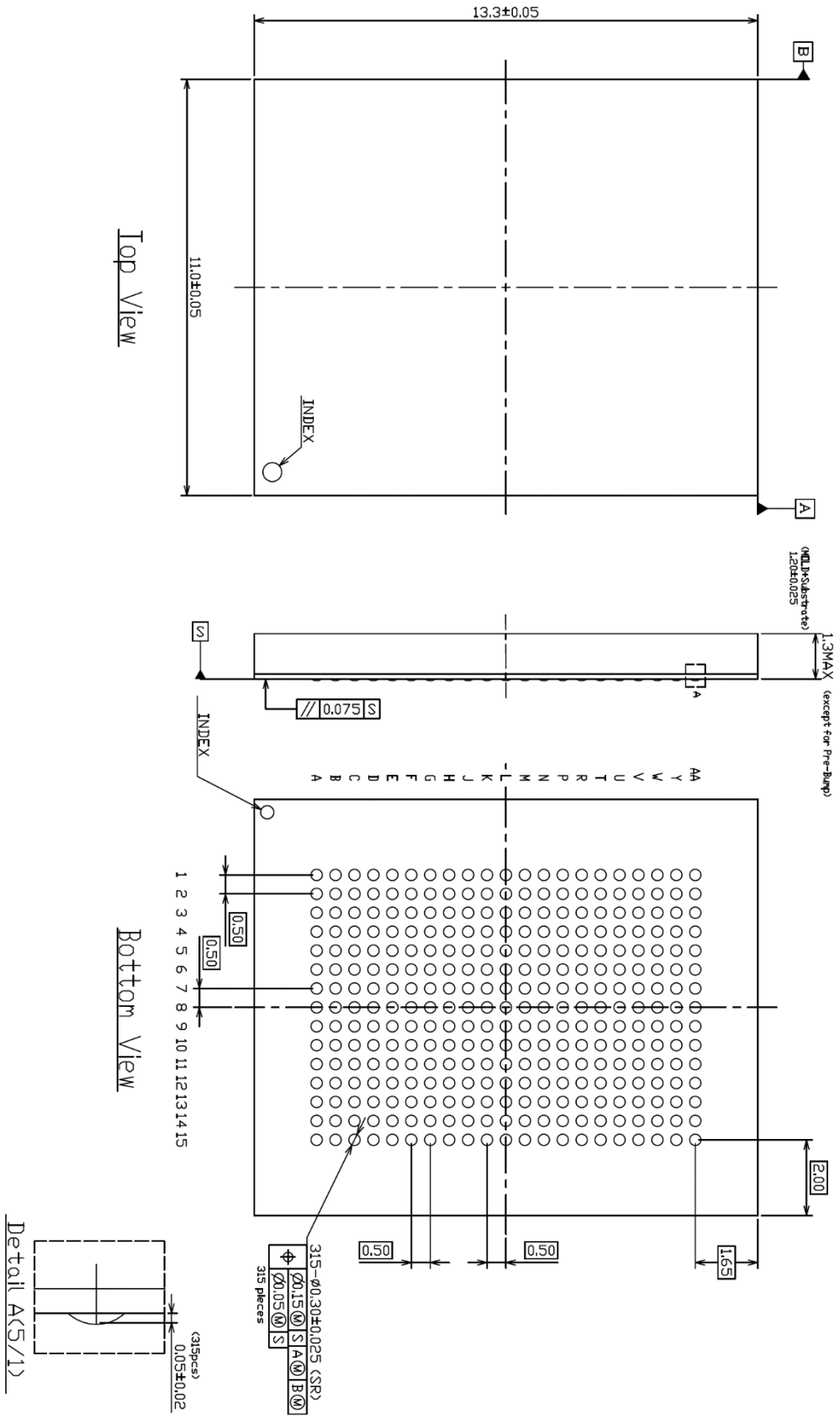

Figure 11 Package Dimension of P-FLGA315-1114-0.50-001

Table 40 Typical net weight of S5E+BiCS5 MCP device

KIOXIA's Part Number	Memory Die Type	Density	z-height	Typical Net weight
THGBY8G9A15LFAN	BiCS5 512Gb iTLC3	64GB	0.87mm	0.220 g/pc
THGBY8T0A25LFAN		128GB		0.220 g/pc
THGBY8T1A45LFAN		256GB		0.225 g/pc
THGBY8T2A85LFAN		512GB	0.9mm	0.225 g/pc
THGBY8T3AB5LFAP		1TB	1.3mm	0.400 g/pc

9 Device Marking

Figure 12 shows the Kioxia S5E+BiCS5 MCP device marking image.

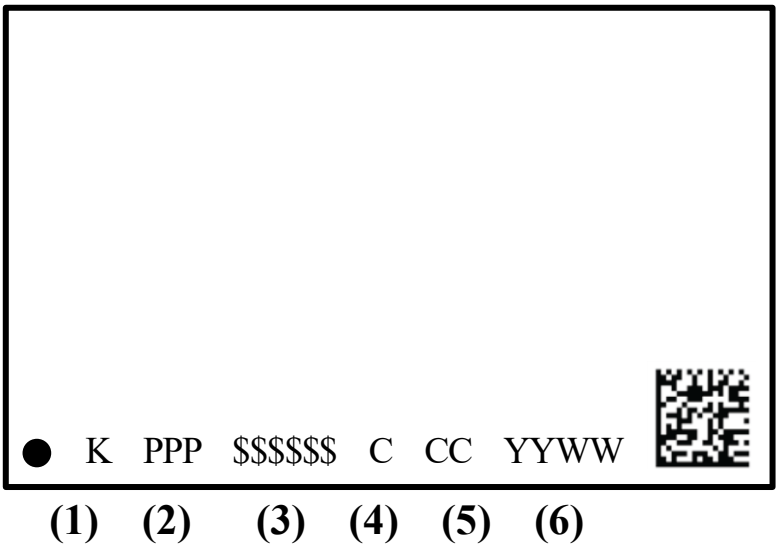

Figure 12 S5E+BiCS5 MCP Device Marking image

Table 41 Device Marking Description

No.	Item	Comments
(1)	Vendor Name	1 digit; K: KIOXIA
(2)	Device Code	3 digits; Represents KIOXIA Part Number THGBY8G9A15LFAN (64GB/1DP) → 5A2 THGBY8T0A25LFAN (128GB/2DP) → 5A3 THGBY8T1A45LFAN (256GB/4DP) → 5A4 THGBY8T2A85LFAN (512GB/8DP) → 5A5 THGBY8T3AB5LFAP (1024GB/16DP) → 5A8
(3)	Key Number	6 digits; KIOXIA internal control code
(4)	Country of Assembly	1 digit; J (Japan) C (China) T (Taiwan)
(5)	Controller HW Version	2 digits; A1
(6)	Weekly Code	4 digits; YY : YY means lower two digits of the year. WW : WW is weekly code. (Weekly code complies with EIA standard)
(7)	2D Barcode	17 digits; It can be expressed with PPPYWWDSSSSEEEERX by using mnemonic described in Table 42.

Table 42 2D Barcode Description

mnemonic	digit	Description	Format	Arbiter	Specification
PPP	17th-15th	Plant/Vender code	Alphanumeric	Apple	PPP means Plant/Vender code. The value is depending on the assembly site of samples. In case of YOK assembly the value shall be “DKG”. In case of PTI assembly the value shall be “FRK”. In case of AMK assembly the value shall be “FQ6”
Y	14th	Year of manufacture code	Numeric	KIOXIA	Y means the lower digit of the year. The value fall in the range of 0 to 9.
WW	13th-12th	Week of manufacture code	Numeric	KIOXIA	WW is weekly code. The value fall in the range of 01 to 53. Sunday shall be the start day of a week. The value is reset to 01 on the first Sunday of January
D	11th	Day of the week code	Numeric	KIOXIA	D is the Day of the week code. The value fall in the range of 1 to 7. Sunday shall be 1. Monday is 2. Saturday will be 7.
SSSS	10th-7th	Sequential count code	Alphanumeric	KIOXIA	SSSS means sequential count code. The value fall in 0000 to ZZZZ per day. The sequential count code ensure the complete 17 digit character serial number is unique.
EEEE	6th-3rd	Engineering configuration code	Alphanumeric	Apple	EEEE means engineering configuration code. There is one to one corresponding between MPN and this code. The relations refer to Table 2 This code plays a role of the unique counter for the Sequential count code described above.
R	2nd	Revision	Alphanumeric	Apple	R means Revision code. The value on the samples graded WS and ES shall be numeric in specification. It starts from “0” and it shall be incremented according to the customer’s request. The increment rule is as follows. 0=>1=>2=>3 ・・・ The value on the samples graded CS, GS and MP shall be alphabet in specification. It starts from “A” and it should be incremented according to the customer’s request. The increment rule is as follows. A=>B=>C ・・・
X	1st	Checksum character	Alphanumeric	KIOXIA	X means Checksum Character. The algorithm is based on Modulo 34.

Figure 13 and Table 43 show the S5E+BiCS5 MCP device 2D Barcode drawings and dimensions.

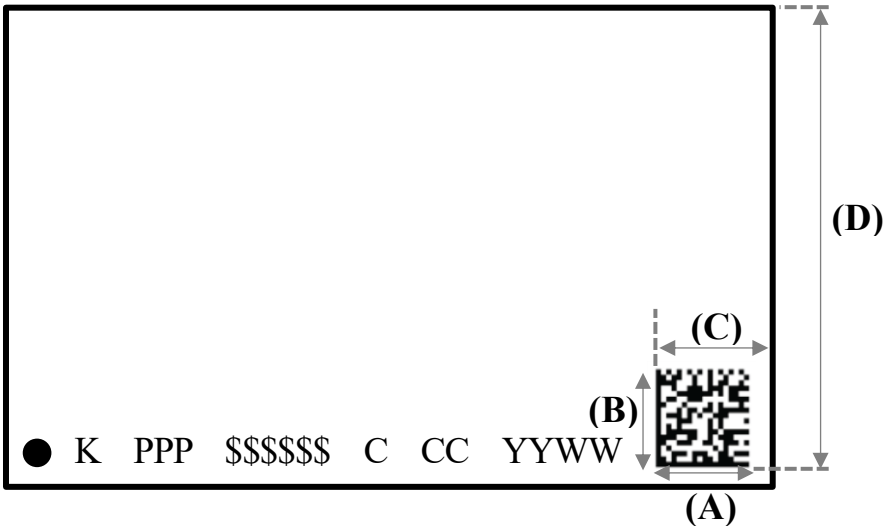

Figure 13 S5E+BiCS5 MCP device 2D Barcode drawings

Table 43 2D Barcode Dimensions

No.	Item	Dimensions (typical)	
		Micro Package	Mini Package
(A)	2D Barcode width	2.16 [mm]	2.16 [mm]
(B)	2D Barcode height	2.16 [mm]	2.16 [mm]
(C)	Offset from left edge	2.56 [mm]	2.56 [mm]
(D)	Offset from bottom edge	8.60 [mm]	10.60 [mm]

Revision History

Date	Rev.	Description
Feb.2nd, 2022	1.0	- Initial Release
Mar.2nd, 2022	1.1	- Revised Kioxia Part Number on Table 2 - Added 16-digit of Kioxia Part Number (AMK with AT2 Au wire) on Table 1 and Table 2
		-

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