64/128/192/256/320/512/1024GB

E3NAND_M14 Fab

64GB : HN3G9DT1CAX372, HN3G9DT1CAX378

128GB : HN3T0DT2CAX373, HN3T0DT2CAX379

256GB : HN3T1DT4CAX375, HN3T1DT4CAX381

512GB : HN3T2DT8CAX384, HN3T2DT8CAX383

1024GB :HN3T3DTGCAX410, HN3T3DTGCAX411

E3NAND_M15 Fab

64GB : HN3G9DT1CAX385, HN3G9DT1CAX392

128GB : HN3T0DT2CAX386, HN3T0DT2CAX393

256GB : HN3T1DT4CAX388, HN3T1DT4CAX395

512GB : HN3T2DT8CAX390, HN3T2DT8CAX397

1024GB : HN3T3DTGCAX421, HN3T3DTGCAX420

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Document Title
64/128/256/512/1024GB E3NAND Specification

Revision History

Table1. Document Revision History

Revision No.	History	Draft Date
0.0	-. Draft version	Apr. 13. 2021
0.1	-. 1024GB 0.9T added & 192/320GB deleted	Nov. 23. 2021
0.2	-. Updated package outline drawings	Dec. 03. 2021
0.3	-. 1024GB 1.3T added	Dec. 10. 2021
0.4	-. Key features /appendix updated	May. 23. 2022
0.5	-. 3DV7 512Gb S5E from M15 Fab added	Jun. 23. 2023
0.6	-. Package Pin Layout Resolution Improved	Apr. 19. 2024

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1. Introduction

1.1. Goals and Objectives

This document communicates the specification for E3NAND

1.2. Key Features

■ Physical Interface
- PCIe Gen4

■ Memory Technology
- 512Gb 3bit per cell

■ E3NAND Organization
- 64GB : 1+1-stacks
- 128GB : 1+2-stacks
- 256GB : 1+4-stacks
- 512GB : 1+8-stacks
- 1024GB : 1+16-stacks

■ Power Supply
- VDD for high VDD operational mode : 0.845~0.94V
- VDD for low VDD operational mode : 0.78~0.9V
- VCCQ for high VCCQ operational mode : 1.7~1.95V
- VCCQ for low VCCQ operational mode : 1.14~1.3V
- VCC : 2.35~2.75V

■ Net Weight
- 64GB : 0.216[g]
- 128GB : 0.218[g]
- 256GB : 0.218[g]
- 512GB : 0.228[g]
- 1024GB : 0.289[g]

■ Package
- 64/128/ 256GB : LGA315 (09.0 x 13.3 X 0.87mm)
- 512GB : LGA315 (09.0 x 13.3 X 0.9mm)
- 1024GB : LGA315 (11.0 x 13.3 X 0.9mm)

■ FW version
- PTS 17

■ E3NAND controller version
- S5E A1

■ Operation Temp
- Case surface temperature (-15~85C)

1.3. Product List

1.3.1. Part number

Part Number	VDD	VDDIO	VCC	Organization	Density	B/E site
HN3G9DT1CAX372	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 1	64GB	CJ
HN3G9DT1CAX378	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 1	64GB	CQ
HN3T0DT2CAX373	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 2	128GB	CJ
HN3T0DT2CAX379	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 2	128GB	CQ
HN3T1DT4CAX375	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 4	256GB	CJ
HN3T1DT4CAX381	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 4	256GB	CQ
HN3T2DT8CAX384	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 8	512GB	CJ
HN3T2DT8CAX383	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 8	512GB	CQ
HN3T3DTGCAX410	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 16	1024GB	CJ
HN3T3DTGCAX411	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 16	1024GB	CQ
HN3G9DT1CAX385	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 1	64GB	CJ
HN3G9DT1CAX392	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 1	64GB	CQ
HN3T0DT2CAX386	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 2	128GB	CJ
HN3T0DT2CAX393	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 2	128GB	CQ
HN3T1DT4CAX388	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 4	256GB	CJ
HN3T1DT4CAX395	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 4	256GB	CQ
HN3T2DT8CAX390	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 8	512GB	CJ
HN3T2DT8CAX397	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 8	512GB	CQ
HN3T3DTGCAX421	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 16	1024GB	CJ
HN3T3DTGCAX420	0.835/ 0.9V	1.23/ 1.8V	2.5V	1 + 16	1024GB	CQ

1.3.2. Marking Information

No		Code	
1	H	SK hynix	SK hynix
2	N	Product Family	Flash
3	3	Product Mode	Customized
4,5	G9 T0 T1 GQ GS T2 GV GT T3 TA	Product Density	G9 : 64GB T0 : 128GB GP : 192GB T1 : 256GB GQ : 320GB GS : 384GB T2 : 512GB GV : 576GB GT : 640GB T3 : 1TB
6	8 9 A B C D E	NAND Info	8 : 3DV4 256G 9 : 3DV4 512G A : 3DV5 512G B : 3DV6 512G C : 3DV6 1T D : 3DV7 512G
7	T	Cell Type	TLC
8	1 2 3 4 5 6 8 9 A G	Number of Die	1 : SDP 2 : DDP 3 : TDP 4 : QDP 5 : 5DP 6 : 6DP 8 : ODP 9 : 9DP A : 10DP G : 16DP
9	A B C	Controller Name	A : S3E B : S4E C : S5E
10	A	Client Name	Apple
11	X	Reserved	
12			
13	Combination Code		
14			

2. Physical Interface

2.1. Package Pin Layout

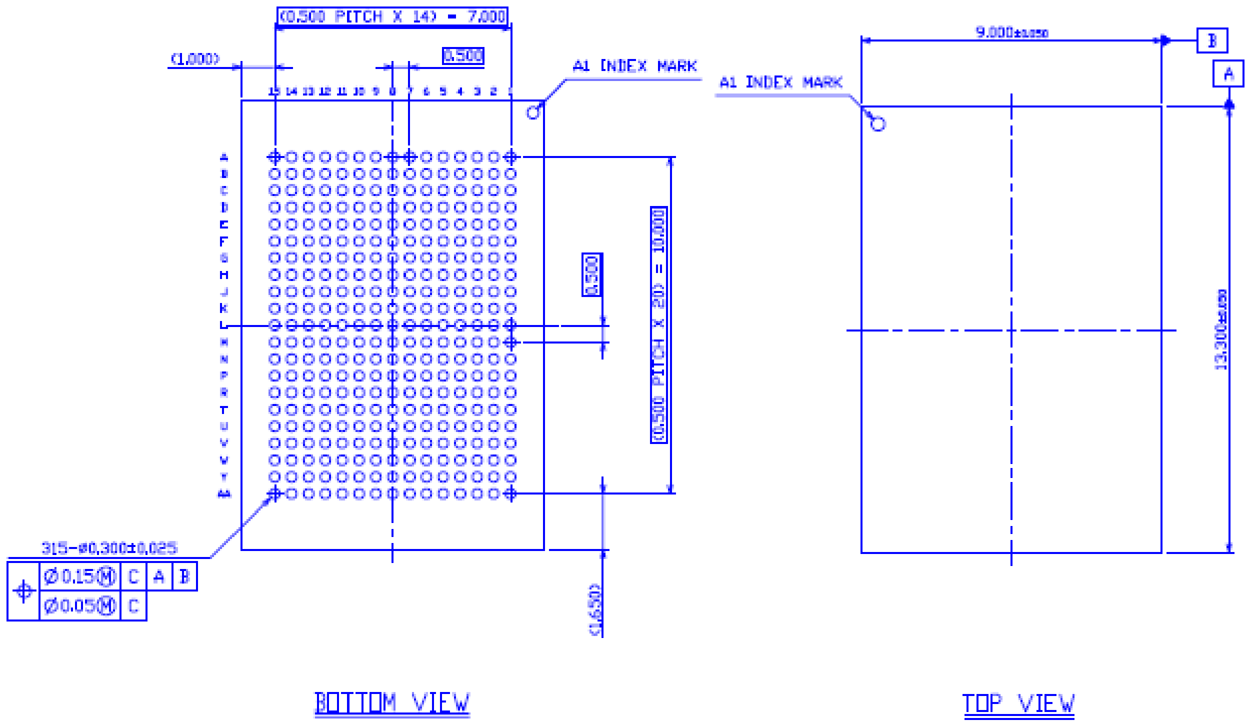
The S5E LGA has 315 pins, with the pin list and layout as shown below

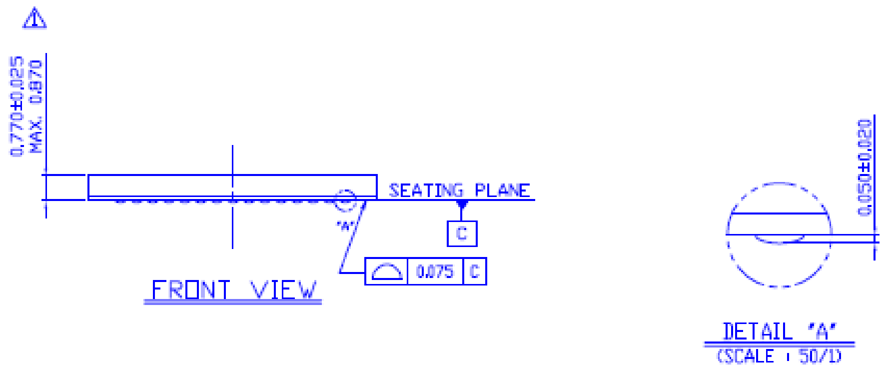
	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	1
2	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	2
3	Dummy	Dummy	Dummy	Dummy	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	Dummy	Dummy	Dummy	3
4	Dummy	Dummy	Dummy	VSS	VCC	VCC	VDDIO_2_L_ANI	VDDIO_2_L_ANI	DROOP_N	VDDIO_2_DP	VDDIO_2_DP	VDDIO_2_L_ANI	VSS	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VCC	VCC	RFU_2	VSS	Dummy	Dummy	4
5	VSF	Dummy	Dummy	VSS	VSS	VSS	VDDIO_1	VDDIO_1	VSS	ANI1_VREF	RFU	ZQ_1	VSS	VDDIO_1	VDDIO_1	VSS	WP_N	RFU_2	RFU_2	VSS	VSF	5
6	Dummy	Dummy	Dummy	VSS	PCIE_REFCLK_N	PCIE_REFCLK_P	VSS	PCIE_CLKREQ_N	AVDD1X_PLL	VDD_PLL	RFU	RFU	RESETN	VQPS	EXT_RNB	EXT_NWE	EXT_NRE	RFU_2	RFU_2	VSS	Dummy	6
7	Dummy	Dummy	Dummy	VSS	VSS	VSS	PCIE_VDD	PCIE_VDD	VDD	VDD	VSS	VDD	VDD	VSS	EXT_CLE	TRSTN	EXT_ALE	RFU_2	RFU_2	VSS	Dummy	7
8	Dummy	Dummy	Dummy	VSS	PCIE_RX0_P	PCIE_RX0_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	EXT_D0	EXT_D2	EXT_D3	RFU_2	RFU_2	VSS	Dummy	8
9	Dummy	Dummy	Dummy	VSS	VSS	VSS	PCIE_VDD	PCIE_AVDD_H	VDD	VDD	VSS	VDD	VDD	EXT_D1	EXT_D4	EXT_D6	EXT_D5	RFU_2	RFU_2	VSS	Dummy	9
10	Dummy	Dummy	Dummy	VSS	PCIE_TX0_P	PCIE_TX0_N	VSS	PCIE_AVDD_H	PCIE_RESREF	RFU	RFU	RFU	RFU	RFU	EXT_D7	EXT_NCE	EXT_DQS	RFU_2	RFU_2	VSS	Dummy	10
11	VSF	Dummy*	Dummy	VSS	VSS	VSS	VDDIO_1	VDDIO_1	CLK_IN	ZQ_0	RFU	ANI0_VREF	VSS	VDDIO_1	VDDIO_1	VSS	VPP	RFU_2	RFU_2	VSS	VSF	11
12	Dummy	Dummy	Dummy	VSS	VCC	VCC	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VSS	VDDIO_2_L_ANI	VDDIO_2_DP	VDDIO_2_DP	VSS	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VCC	VCC	RFU_2	VSS	Dummy	Dummy	12
13	Dummy	Dummy	Dummy	Dummy	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	Dummy	Dummy	Dummy	13
14	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	14
15	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	15

Figure 1: S5E Mk2 Package LGA315 Pin Assignment

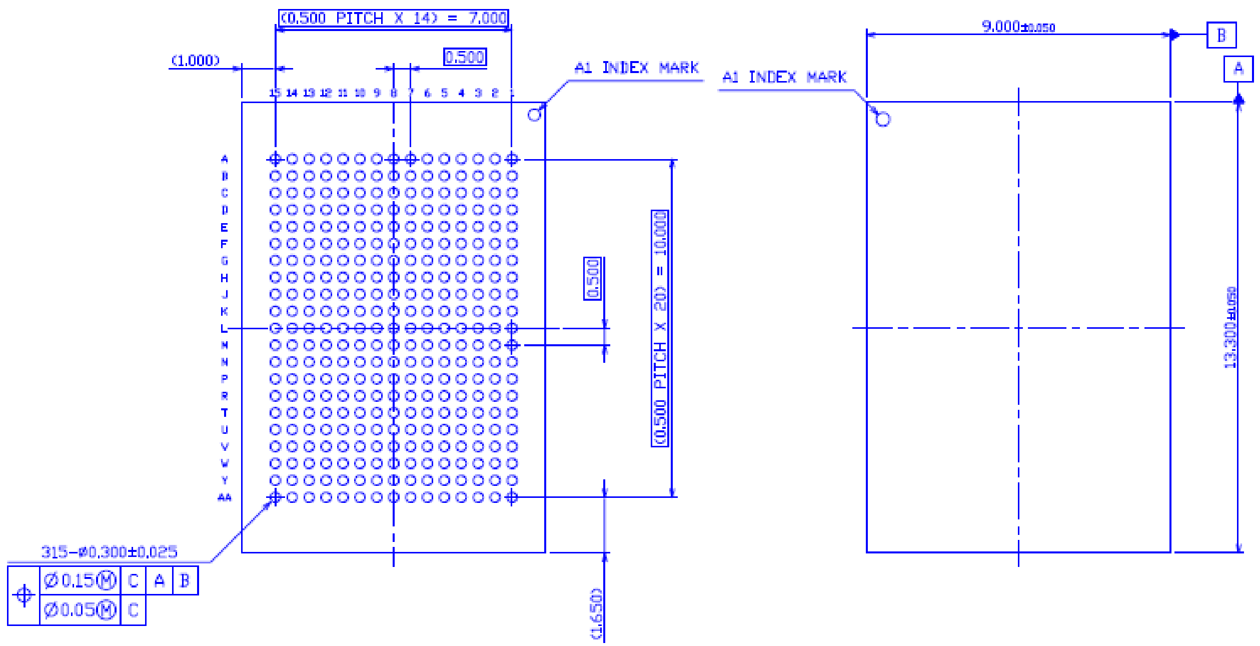
Package Pins	Usage in package	Comment
VDDIO_2_L_ANI	Same as VDDIO_2 in legacy PKG	NAND IF IO supply
VDDIO_2_DP	Same as VDDIO_2 in legacy PKG Merged with VDDIO_2_L_ANI	Included in VDDIO_2_L_ANI for SIPI purpose *May separate beyond Mk2 package
RFU	Floating individually	Reserved for Future Use
RFU_2	Floating individually	Reserved for Future Use
Dummy	Tied to VSS	
Dummy*	Floating	*Y11 pin
VSF	- If vendor doesn't use VSF, these pins shall be shorted to VSS in package substrate - If vendor implement VSF connection to NAND die(s), 1. Vendor shall provide pre-notification and function of the pins to Apple, and need Apple approval before implementation 2. These pins in NAND die user mode shall be self-pulldown to VSS, or shall keep stable high-Z with characteristics confirmed with Apple 3. These pins in NAND die user mode shall be allowed to float or short to VSS, in Apple side usage 4. These pins also shall comply with ESD specifications	Vendor Specific Feature *A5, A11, AA5, AA11 pins

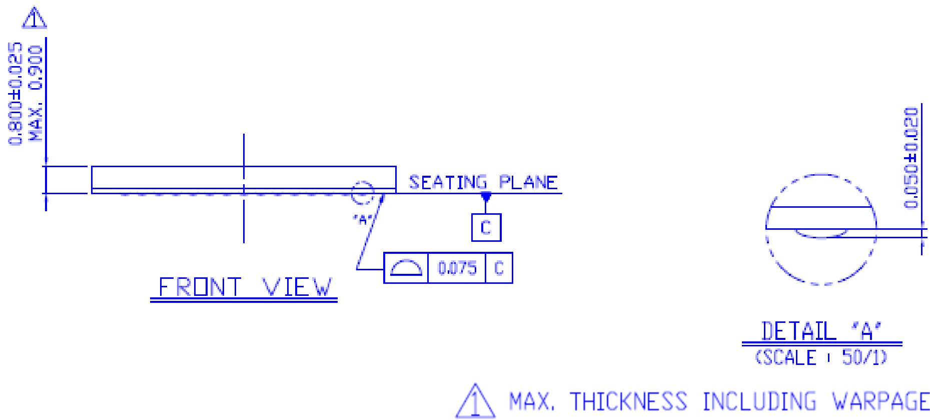
Number of NAND stack	X (mm)	Y (mm)	Z max (mm)	Body THK (mm)	Pre-bump (㎛)
1 / 2 / 4 die	13.3 (±0.05)	9.0 (±0.05)	0.87	0.77 (±0.025)	50 (±20)
8 die	13.3 (±0.05)	9.0 (±0.05)	0.9	0.8 (±0.025)	
16 die	13.3 (±0.05)	11.0 (±0.05)	0.9	0.8 (±0.025)	



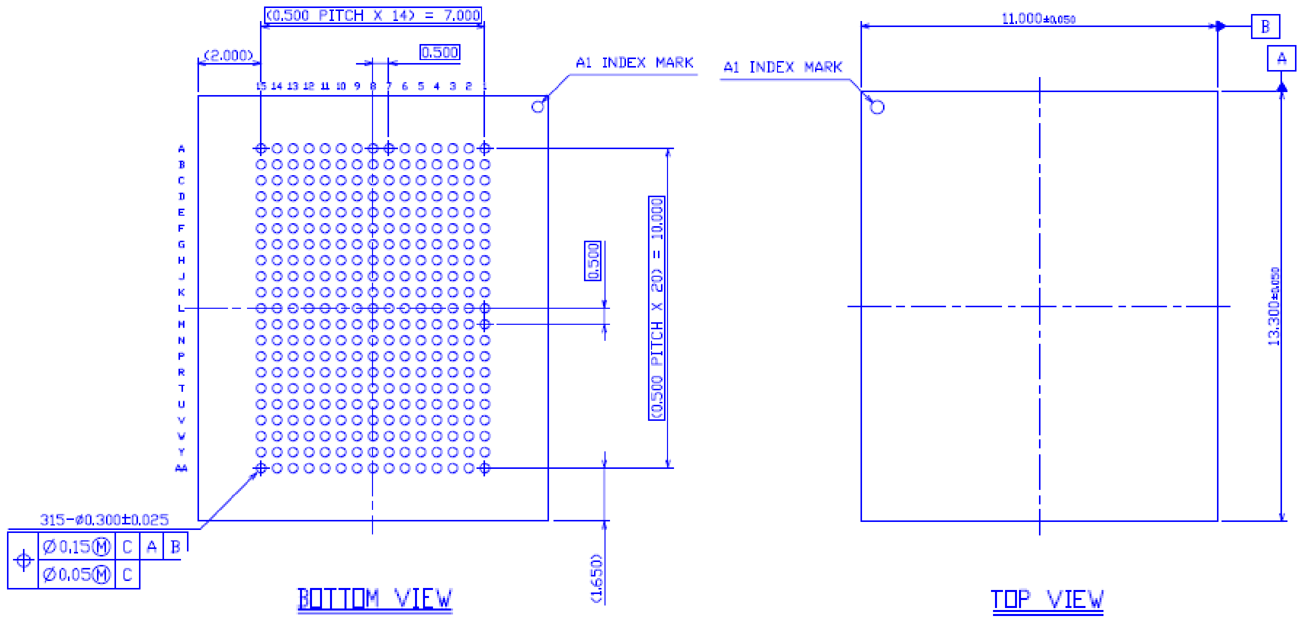


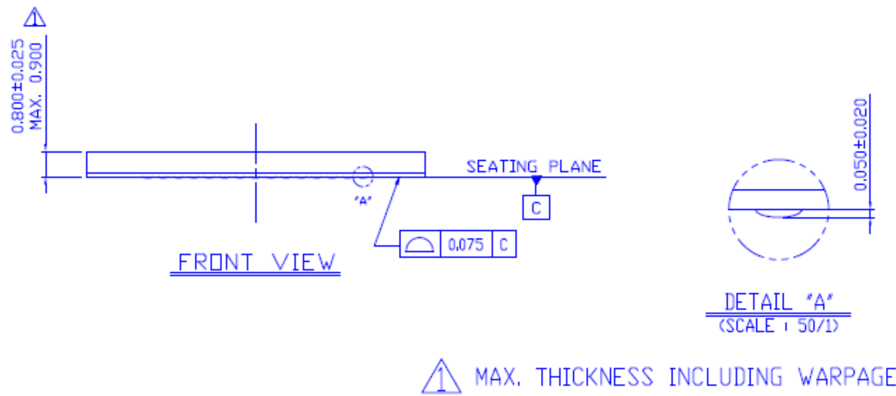
13.3x9.0x0.87mm LGA315 Package Outline Drawing





13.3x9.0x0.9mm LGA315 Package Outline Drawing





13.3x11.0x0.9mm LGA315 Package Outline Drawing

Appendix A. The keeping condition

1) The keeping condition before open the dry packing.
   12 month, < 40°C / 90%RH below.

2) The keeping condition after open the dry packing.
   30 °C / 60%RH below it has to use within 168hrs after open the dry packing or Stored at < 20%RH.

3) It's necessary to bake in case of using after 168hrs opened the day packing.

   Bake condition
   - Tube : 125 °C / 5hrs
   - Tape & reel : 40°C / 192hrs, Do not over 50°C.
   - Reflow is allowed by 4 times after bake in the condition above.

4) If you have using the device within 168hrs after open the dry packing,
   the others will be keeping by Re-dry packing. (This device also allows 4times IR reflow.)

5) MSL(Moisture Sensitive Levels) : level 3

Appendix B. Moisture Caution

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

Do not open except under controlled conditions

1. **Calculated shelf life sealed bag**

    12 months at < 40°C and < 90% relative humidity (RH)

2. **After bag is opened,**

    devices that will be subjected to reflow solder or high temperature process must

    a) Mounted within : 168 hours of factory conditions < 30°C / 60%RH, or

    b) Stored at < 20%RH

3. **Devices require bake, before mounting,**

    if Humidity Indicator Card is > 10% when read at 23 ± 5°C

4. **If baking is required,**

    devices may be baked for 192hours at 40°C, < 5%RH or 5hours at 125°C

    Caution : Tape & Reel or tubes will melt at 125°C, Trays must be used at 125 °C