3D NAND Flash: Gen5 X3 512Gb 2-Plane S5E (iTLC3) for Apple

June 23, 2022
Revision 1.5

Marketing Part Numbers

Standard SKUs: FW (TBD)			
SDMVGJLK1-064G	(1-die)	SDSFGJLK1-064G	(1-die)
SDMVGJLK2-128G	(2-die)	SDSFGJLK2-128G	(2-die)
SDMVGJLK4-256G	(4-die)	SDSFGJLK4-256G	(4-die)
SDMVGJLK5-320G	(5-die)	SDSFGJLK5-320G	(5-die)
SDMVGJLK8-512G	(8-die)	SDSFGJLK8-512G	(8-die)
SDMVGJLK9-576G	(9-die)	SDSFGJLK9-576G	(9-die)
SDMVGJLKH-1T00	(16-die)	SDSFGJLKH-1T00	(16-die)

Note 1. For Mk2 information and part numbers, see "3.2 Mk2 Packaging" and Tables 2 and 3, page 8.

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1 Features

Table 1: 3D S5E Gen5 X3 512Gb 2-Plane Features

Feature	Description	
Organization		
Memory cell array per plane	18,336 x 8 bits x 1344 pages x 1662 blocks	
Shared strings	4	NAND strings: 112
Number of planes	2 physical planes per die	
Block size	TLC: 21MB	SLC: 7MB
Page size	18,336 bytes	
Pages per block	1344 pages	
Mode Control		
	Serial input/output, command control	
Modes		
Array-independent modes	**Array-dependent modes***	
ID Read Set/Get Features Status Read Reset operation	Dynamic Read TLC Page Read Cache Read SLC Read	TLC Program Cache Program SLC Program
	TLC Block Erase SLC Erase	
	*These modes are functional in single- or multi-plane operations	
Number of valid blocks (N_{VBD}) per die		
	Min: 3150 blocks	Max: 3324 blocks
Power supply		
	V_{CC}: 2.35–3.6V	V_{CCQ}: 1.14–1.3V (1.2V range) or 1.7–1.95V (1.8V range)
Access time		
Cell array to register (tR)	TLC:	55µs (avg)
	SLC:	34µs (typ)
	Serial Read cycle:	20ns (min)
Toggle Mode data transfer rate	DDR 2.0 Max: (1.8/1.2V range only) 266 MHz (533 Mbps) DDR 3.0 Max: (1.2V range only) 400 MHz (800 Mbps)	DDR 4.0 Max: (1.2V range only) 600 MHz (1200 Mbps)
Legacy data transfer rate	50 MHz (50 Mbps)	
Program/Erase time		
Page Program (typ)	TLC: = typical total programming time for lower + middle + upper page Program completion	1005µs
	SLC: µs per page	1P0V = 60µs, 1P1V = 110µs
Block Erase (typ)	per block	10ms
Operating case temperature		
T_{CASE}	–15°C to 85°C	

Table 1: 3D S5E Gen5 X3 512Gb 2-Plane Features (cont'd)

Feature	Description	
Operating current		
Read (25ns cycle):	TLC: 34mA max[1]	SLC: 35mA max (2 planes)
Program (avg)	TLC: 29mA max[1]	SLC: 25mA max (2 planes)
Erase (avg)	TLC: 15mA max[1]	SLC: 15mA max (2 planes)
Standby:	100µA max per die	
Package		
BGA	110-ball BGA: 1D, 2D, 4D, 5D, 8D	14.6mm × 11.8mm × 0.9mm
	110-ball BGA: 9D, 16D	14.6mm × 11.8mm × 1.3mm
S5E Controller Features		
S5E Controller Characteristic	Parameter	Possible Values
Internal NAND Flash Interface	Number of NAND Flash die connected to S5E controller	8[1]
	Number of CEn to the NAND Flash	8
	NAND type	Supports TLC technology

Note 1. Per physical plane.

2. The maximum die per host-interface channel is 8; maximum per device is 16.

2 The S5E Data Sheet

2.1 Scope

The SanDisk® S5E data sheet provides S5E-specific information, and the SanDisk S5E part adheres to specifications described in the S5E Spec and the System Spec. Any exceptions are noted in this document.

Unless otherwise noted, this data sheet does not repeat information provided in the following documents:

- SanDisk 3D Gen5 X3 512Gb 2-Plane NAND Flash data sheet
- S5E Vendor Product Specification

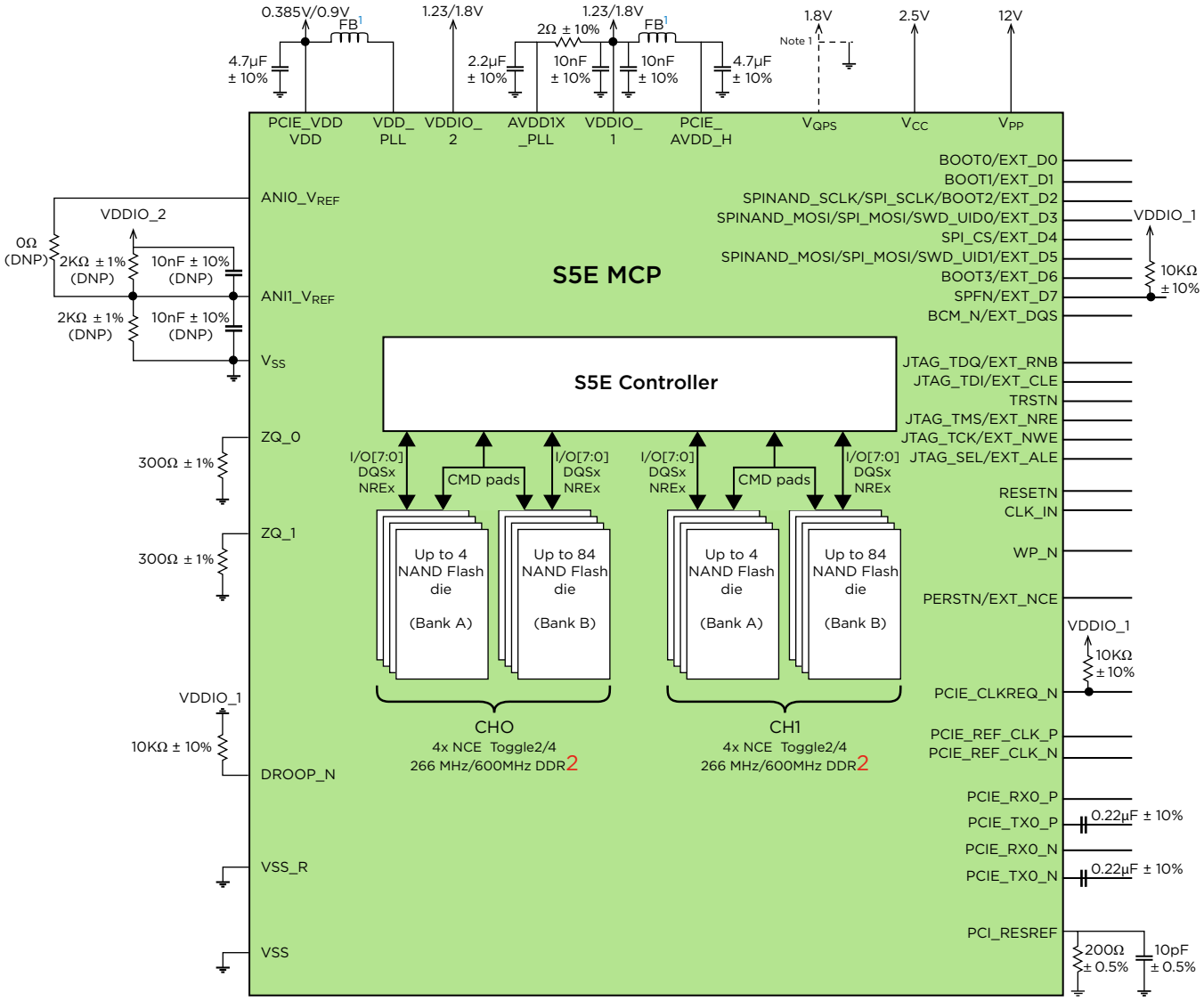
2.2 Overview

The SanDisk S5E 3D Gen5 X3 Flash is a managed NAND solution using the PCIe bus as an external interface. The S5E device is responsible for data reliability in the NAND Flash memory, and no ECC engine is required on the host side.

Each SanDisk S5E part contains an S5E controller connected to an array of SanDisk 3D Gen5 X3 512Gb 2-Plane S5E devices. Detailed information regarding SanDisk NAND Flash memory is provided in the data sheet referenced in the first bullet above.

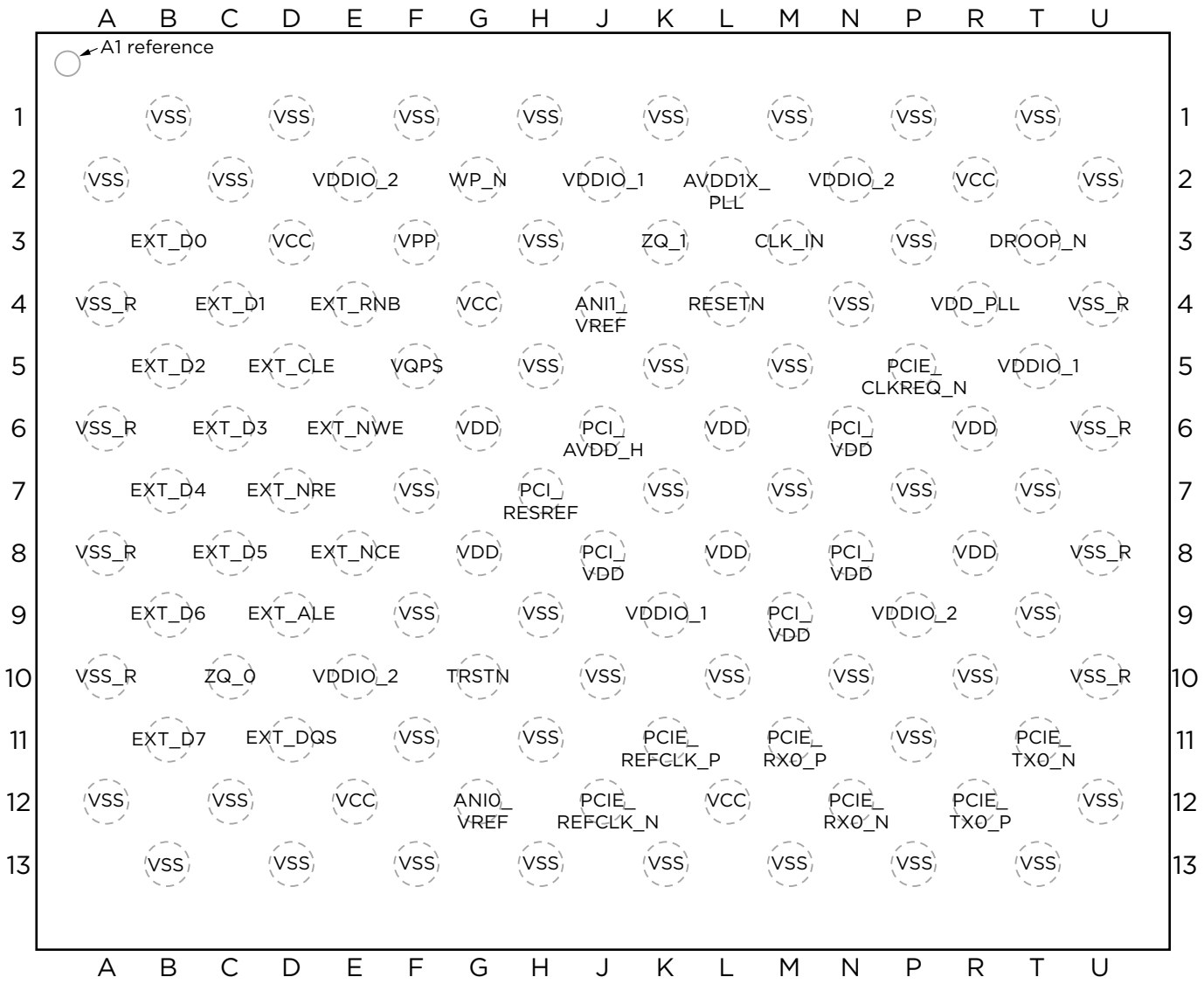
3 Physical Device Interface

Figure 1: Block Diagram: S5E-to-NAND Interface and Host-to-MCP



Note 1. FB = Ferrite bead (from the vendor spec)

Figure 2: 110-Ball BGA Assignments—Top View, Pads Down



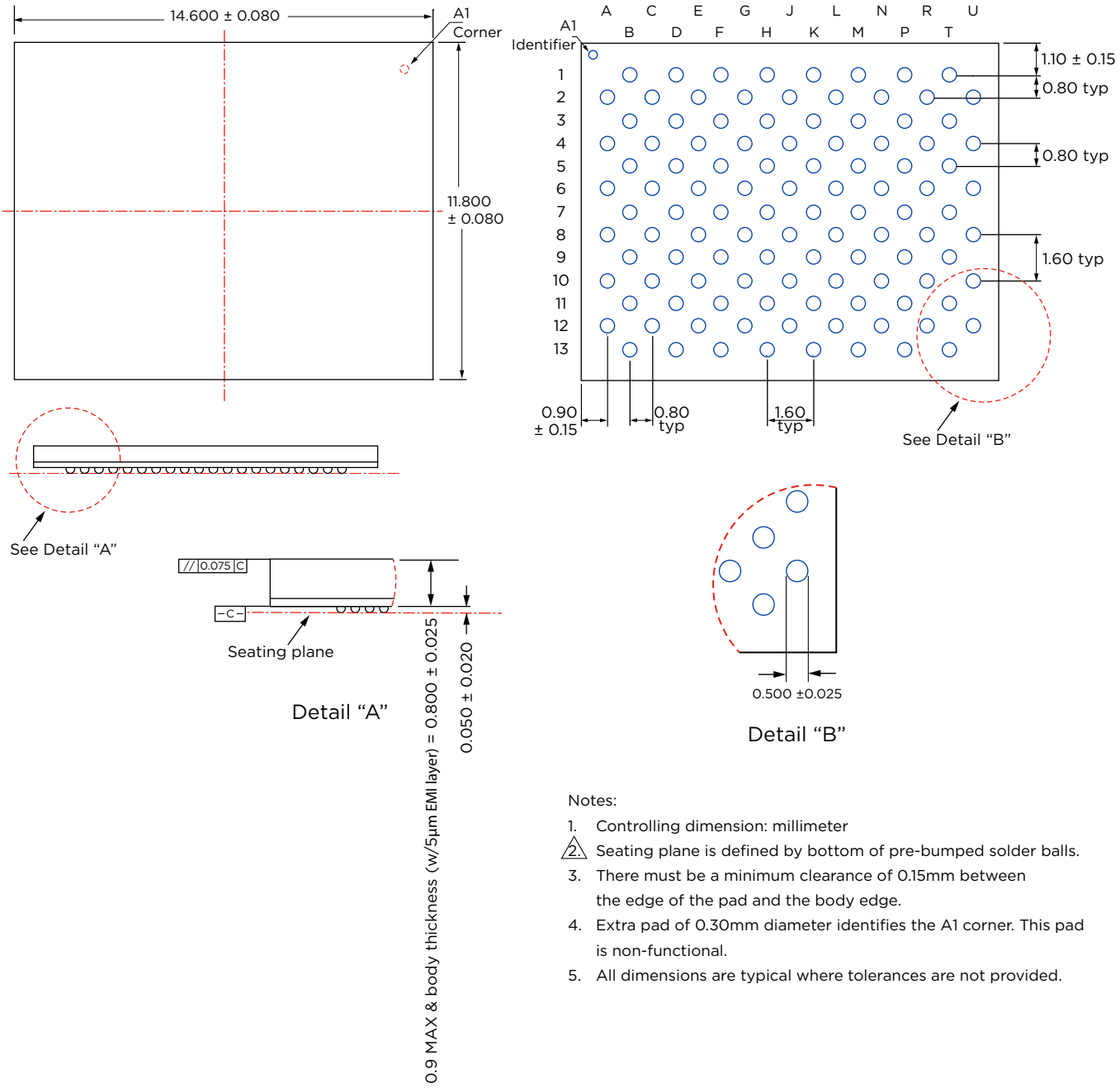
Note 1. This package is designed for mounting on the PCB with underfill. It will not meet board-level (TCT/mechanical shock/vibration) requirements without underfill.

2. If additional, package-related information is required for this product, contact your SanDisk representative.

3.1 Standard Packaging

3.1.1 Standard Package Outline Drawings

Figure 3: Package Outline Diagram: 1-Die, 2-Die, 4-Die, 5-Die, and 8-Die Stacks



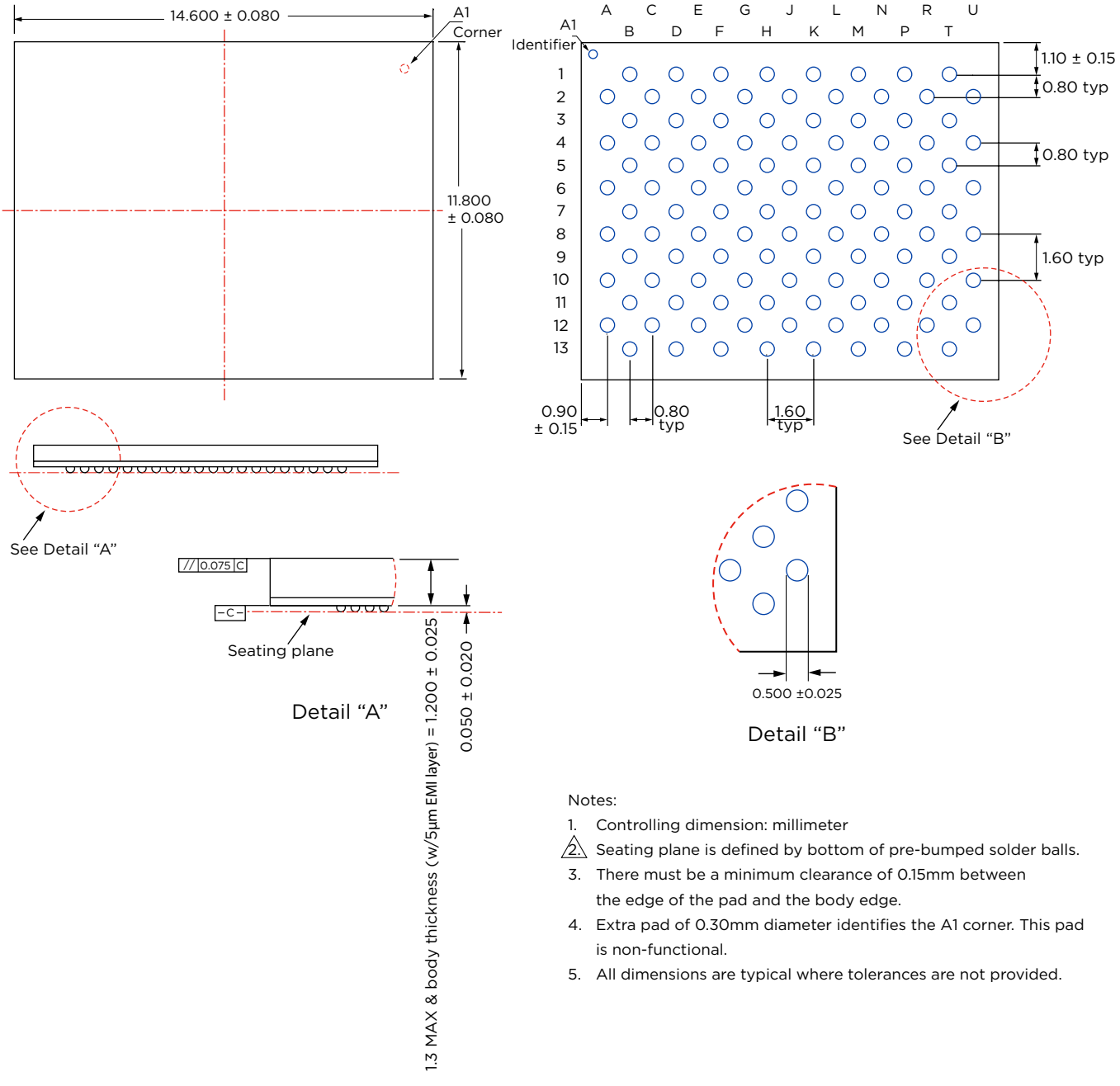
Notes:

1. Controlling dimension: millimeter
2. Seating plane is defined by bottom of pre-bumped solder balls.
3. There must be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. Extra pad of 0.30mm diameter identifies the A1 corner. This pad is non-functional.
5. All dimensions are typical where tolerances are not provided.

Note 1. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.

2. For additional package-related information, contact your SanDisk representative.

Figure 4: Package Outline Diagram: 9-Die and 16-Die Stacks



Notes:

1. Controlling dimension: millimeter
2. Seating plane is defined by bottom of pre-bumped solder balls.
3. There must be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. Extra pad of 0.30mm diameter identifies the A1 corner. This pad is non-functional.
5. All dimensions are typical where tolerances are not provided.

Note 1. This package is designed for mounting on the PCB with underfill. It will not meet board-level TCT requirements without underfill.

2. For additional package-related information, contact your SanDisk representative.

3.2 Mk2 Packaging

Mk2 MPNs, Pad Assignments, and Package Outline Drawings (PODs) specific to Mk2 devices are now provided together in this section. They were provided previously in the ***Apple Mk2 POD Book*** from SanDisk, for Micro packages (1D, 2D, 3D, 4D, 5D, 8D), and for Mini packages (16D).

This section now includes data and graphics for Thin-Micro packages (8D), as well.

Table 2: Mk2 Package Numbers and Configuration: SDSS SKUs

APN	SDSS MPNs			
	SKU Sub-X	SKU Sub-Y	Type	Die
335S00547	N/A	SDSFGKLK1-064G	Mk2-Micro	1-die
335S00548	SDMVGKLK2-128G	SDSFGKLK2-128G[1]	Mk2-Micro	2-die
335S00549	SDMVGKLK4-256G[1]	SDSFGKLK4-256G	Mk2-Micro	4-die
335S00619	SDMVGKLK2-128G	N/A	Mk2-Micro	2-die
335S00620	N/A	SDSFGKLK4-256G	Mk2-Micro	4-die
335S00550	SDMVGKLK8-512G	N/A	Mk2-Micro	8-die
335S00567	N/A	SDSFGKLKH-1T00	Mk2-Mini	16-die

Note 1. MPNs SDMVGKLK4-256G and SDSFGKLK2-128G will be non-Process-on-Record (non-POR) for all programs, all of Fall ‘22 and beyond.

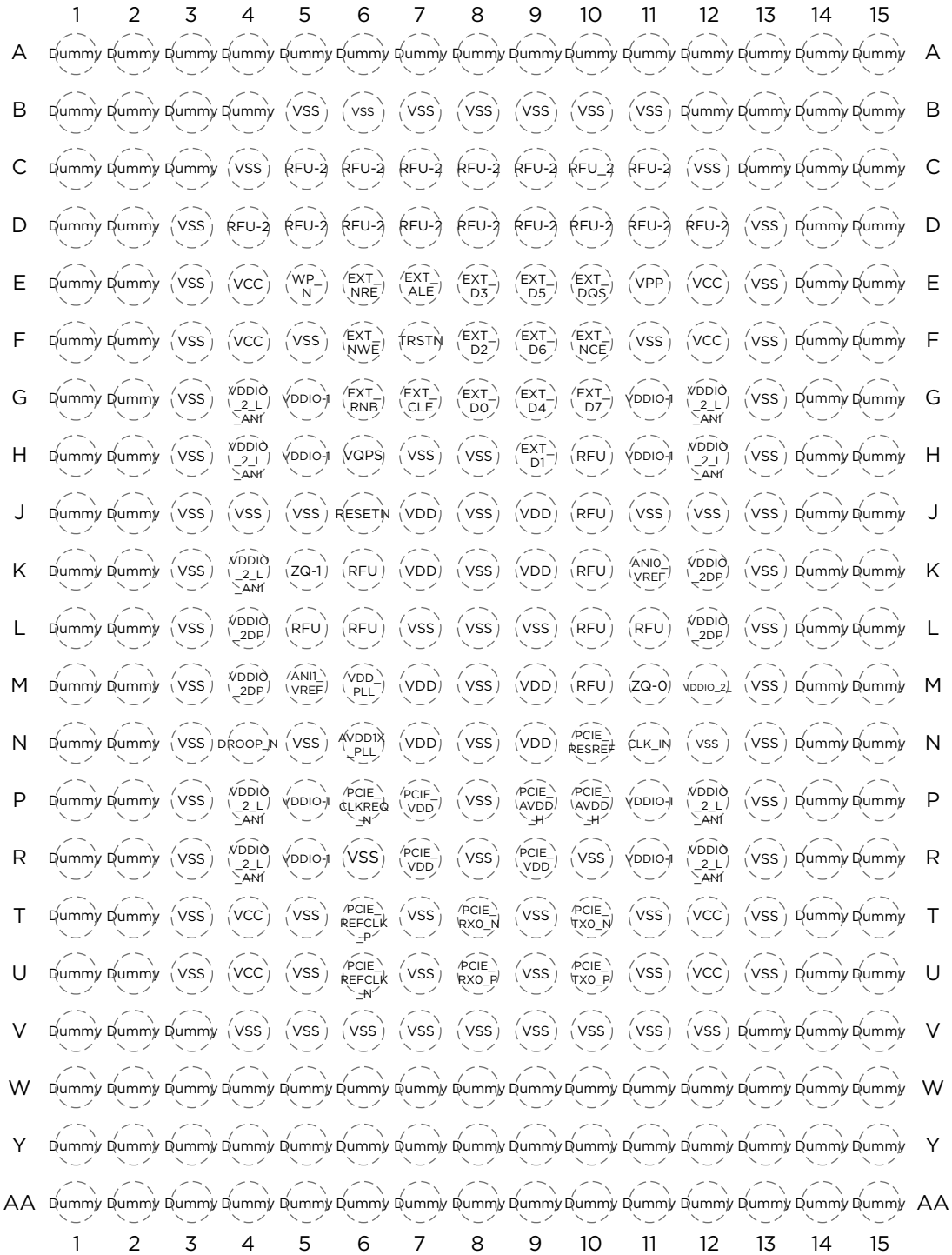
2. APNs 335S00548 and 335S00549 are Spring ‘22 programs.

Table 3: Mk2 Package Numbers and Configuration: SDSM SKUs

APN	SDSM MPNs			
	SKU Sub-X	SKU Sub-Y	Type	Die
335S00619	N/A	SDSMGKLK2-128G	Mk2-Micro	2-die
335S00620	SDMMGKLK4-256G	N/A	Mk2-Micro	4-die
335S00550	N/A	SDSMGKLK8-512G	Mk2-Micro	8-die

3.2.1 MK2 LGA Pad Assignments

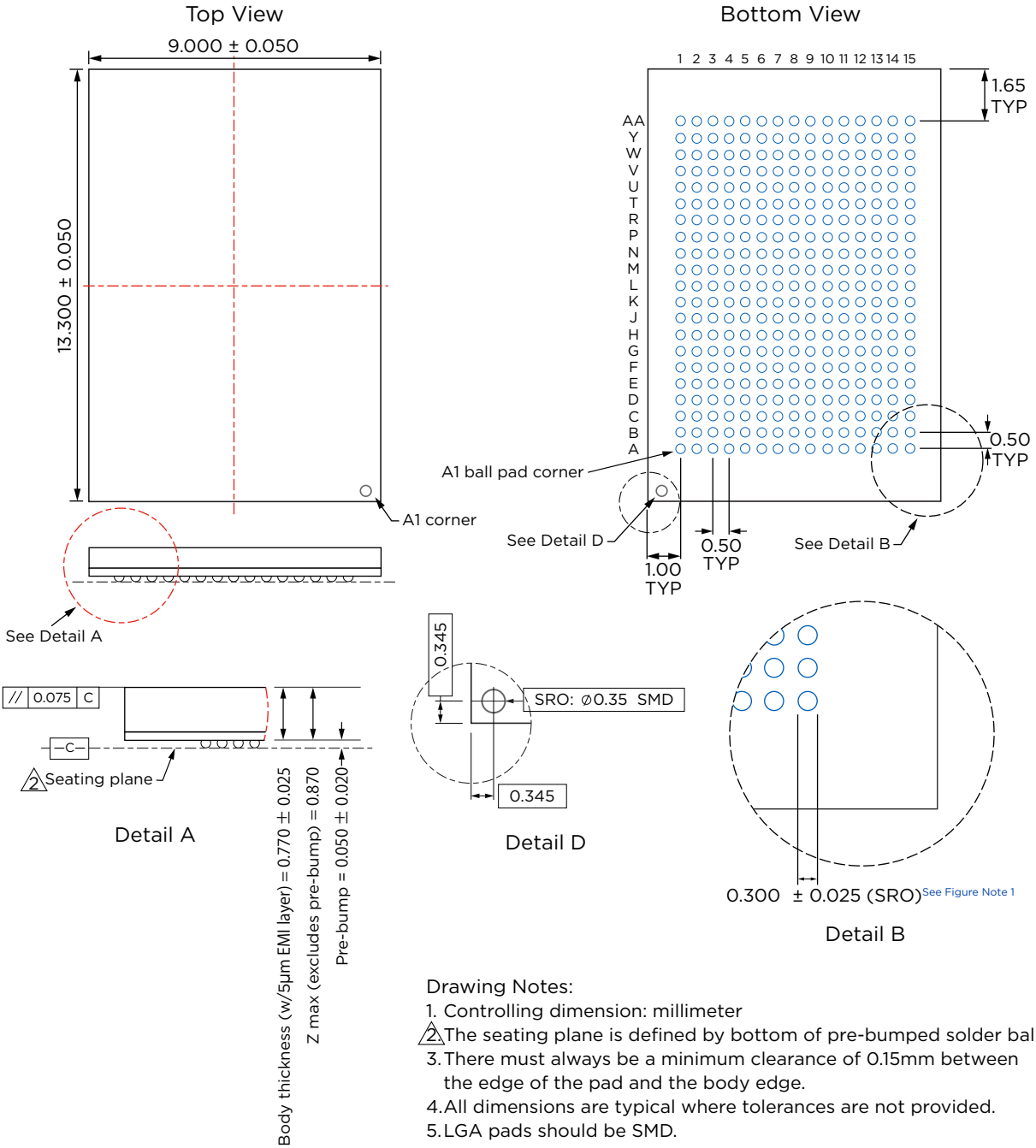
Figure 5: Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments



Pad locations and assignments only; drawing not to scale.

3.3 Mk2 Package Outline Drawings

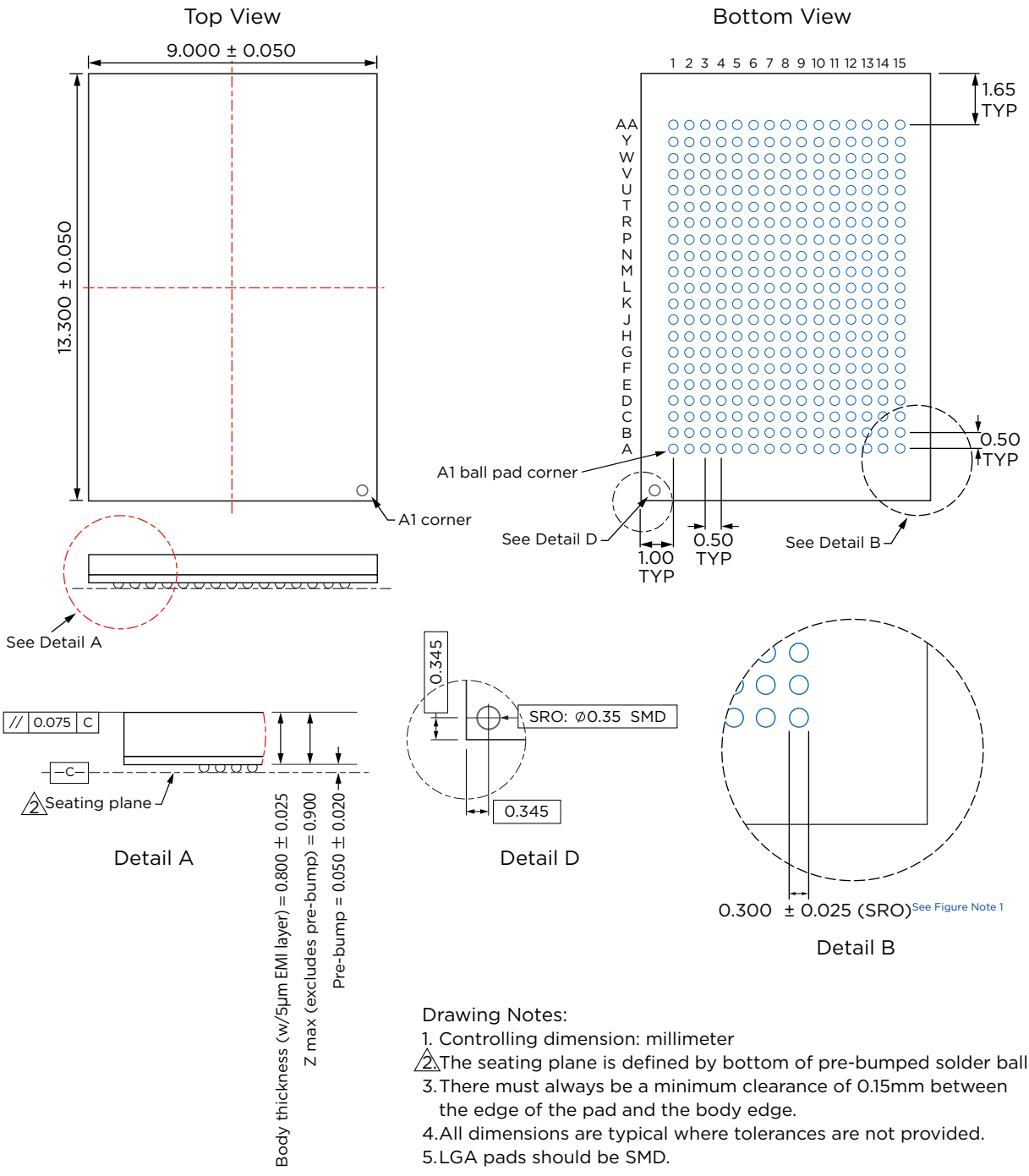
Figure 6: Mk2 Micro: 1-Die to 4-Die Stacks



Drawing Notes:
1. Controlling dimension: millimeter
2. The seating plane is defined by bottom of pre-bumped solder balls.
3. There must always be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. All dimensions are typical where tolerances are not provided.
5. LGA pads should be SMD.

Note 1. See Figure 5, "Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments," on page 9 for PCIE and normal pad assignments.
2. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.
3. For additional package-related information, contact your SanDisk representative.

Figure 7: Mk2 Micro: 5-Die to 8-Die Stacks



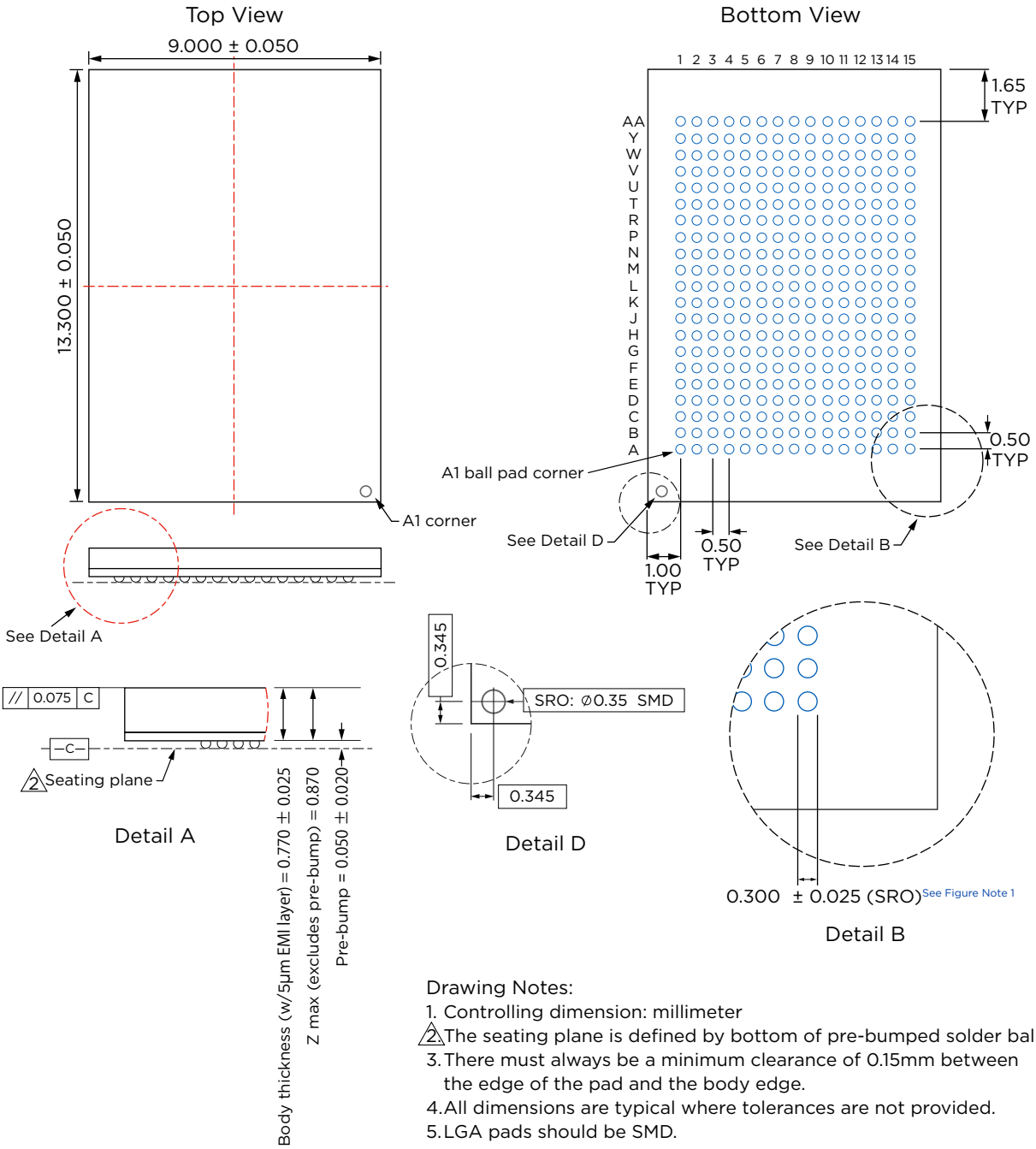
Drawing Notes:

1. Controlling dimension: millimeter
2. The seating plane is defined by bottom of pre-bumped solder balls.
3. There must always be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. All dimensions are typical where tolerances are not provided.
5. LGA pads should be SMD.

Note 1. See Figure 5, "Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments," on page 9 for PCIE and normal pad assignments.

2. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.
3. For additional package-related information, contact your SanDisk representative.

Figure 8: Mk2 Thin Micro: 8 Die (thickness: 0.87µm)



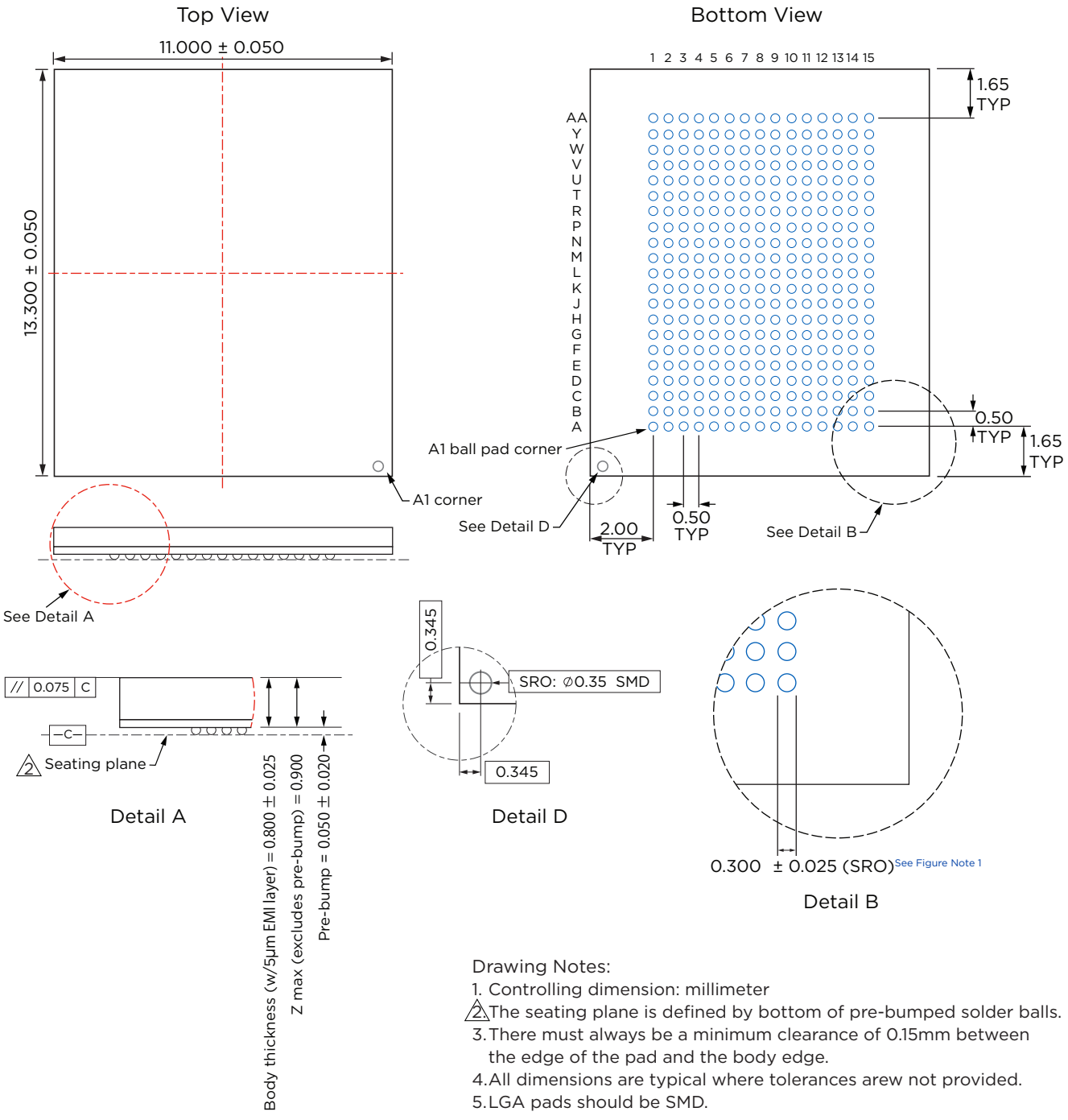
Drawing Notes:

1. Controlling dimension: millimeter
2. The seating plane is defined by bottom of pre-bumped solder balls.
3. There must always be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. All dimensions are typical where tolerances are not provided.
5. LGA pads should be SMD.

Note 1. See Figure 5, “Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments,” on page 9 for PCIE and normal pad assignments.

2. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.
3. For additional package-related information, contact your SanDisk representative.

Figure 9: Mk2 Mini: 5-Die to 8-Die Stacks



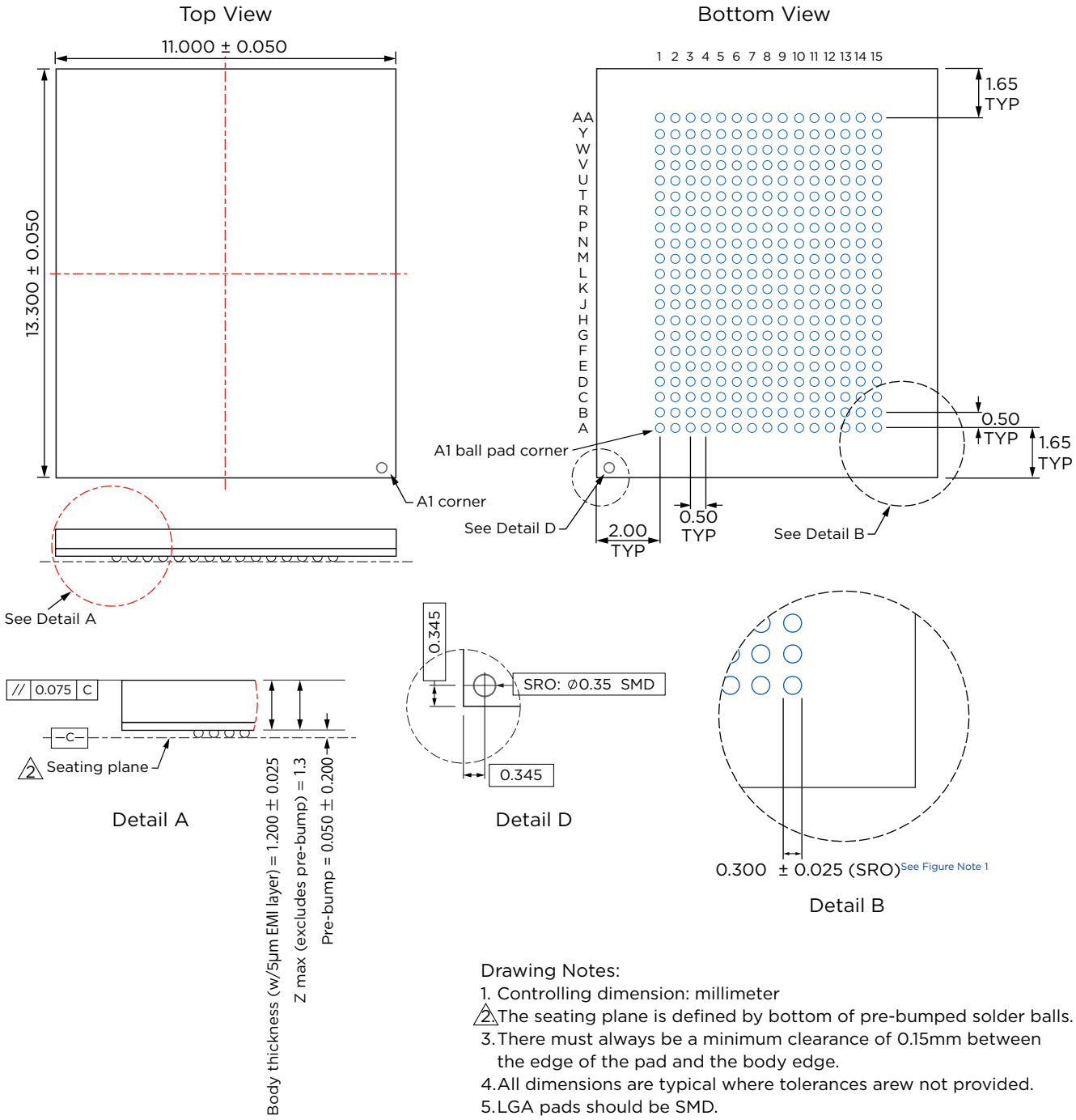
Drawing Notes:

1. Controlling dimension: millimeter
2. The seating plane is defined by bottom of pre-bumped solder balls.
3. There must always be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. All dimensions are typical where tolerances arew not provided.
5. LGA pads should be SMD.

Note 1. See Figure 5, “Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments,” on page 9 for PCIE and normal pad assignments.

2. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.
3. For additional package-related information, contact your SanDisk representative.

Figure 10: Mk2 Mini: 9-Die to 16-Die Stacks



Drawing Notes:

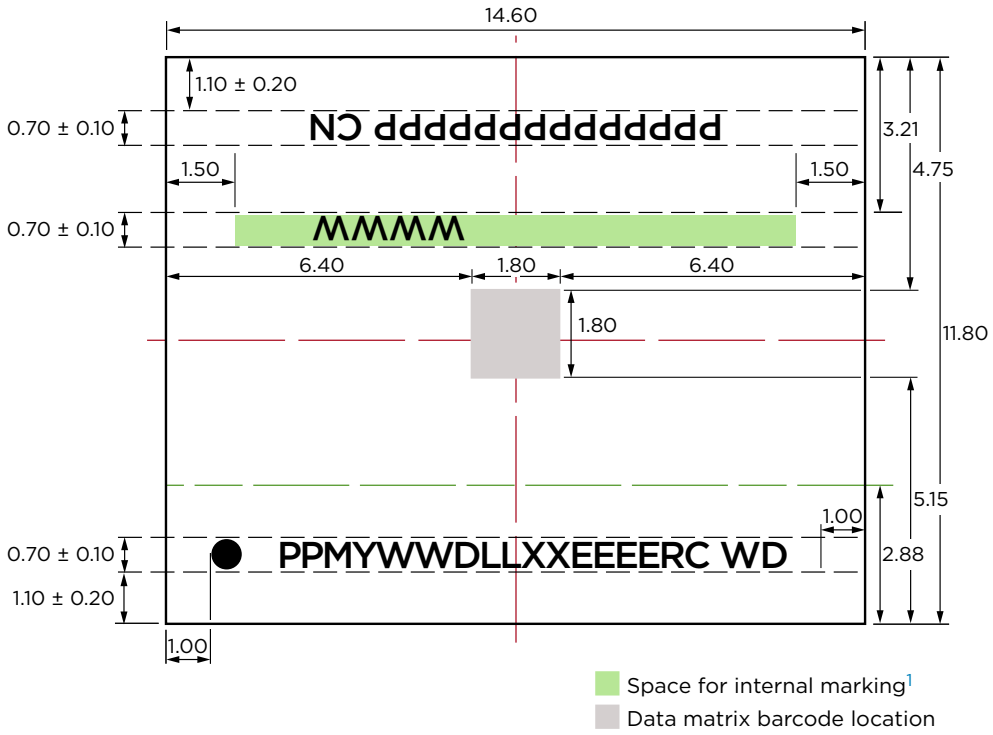
1. Controlling dimension: millimeter
2. The seating plane is defined by bottom of pre-bumped solder balls.
3. There must always be a minimum clearance of 0.15mm between the edge of the pad and the body edge.
4. All dimensions are typical where tolerances arew not provided.
5. LGA pads should be SMD.

Note 1. See Figure 5, "Mk2-Micro, Mk2-Mini, and Mk2-Thin Micro Devices: LGA Pad Assignments," on page 9 for PCIE and normal pad assignments.

2. This package is designed for mounting on the PCB with underfill. It will not meet board-level reliability (TCT/mechanical shock/vibration) requirements without underfill.
3. For additional package-related information, contact your SanDisk representative.

4 Package Marking

Figure 11: Package Marking Diagram



Note 1. For AI sample builds, this space is provided for internal markings, e.g., SBLT/WS/ES/CS.
2. Dimensions are in mm.

4.0.1 Package Marking Requirements

Note 1. Use laser mark.
2. All characters to be legible and complete.
3. Text tolerance:
   ± 0.50mm from center line.
   ± 0.50mm for general text tolerance.
4. PPMYWWDLLXXEEEERC represents the serial number of unit:
   PPM = Plant/Vendor factory code assigned by customer
   Plant code' field of 54-62-XXXXX-XXXG in Agile
   Y = last digit of year
   WW = work week
   D = day of the week, i.e., "1," "2," "3" ..."7"
   M = vendor code per 02-01-WW-02-00010, e.g., SDSS = "D"
   LL = 2-digit MES assembly lot, where L = 1, 2, 3...9 or A, B, C, D...Z (except B, I, O)
   XX = unique ID of each unit, where each X = 1, 2, 3...9 or A, B, C, D...Z (except B, I, O)
   EEEE = Engineering configuration code assigned by customer. Refer to Product Marking
   EEEE Code" field of 54-62-XXXXX-XXXG in Agile

R = Revision code required by customer. Refer to “Product Marking Revision Code” field of 54-62-XXXXX-XXXG in Agile
C = CRC/CKECKSUM digit—auto-generated by laser-marking machine, where C = 1, 2, 3...9 or A, B, C, D...Z (except I, O). Refer to page 2 of this spec

5. 2D barcode content matches serial no. of unit
   2D barcode type: “Data Matrix”
   Size shown: 1.8mm × 1.8mm TYP. Size may vary but must be readable by scanner.
6. Character width = 0.50 ± 0.10mm
7. Character height = 0.70 ± 0.10mm
8. PPPPPPPPPPPPPP represents the product SKU; for example: SDMLSEDF4-064G
   Refer to “Product Marking” field of 54-62/82-XXXXX-XXXG in Agile
   (SKU format is described in 00-02-WW-02-00004)
9. For all sample builds, must add WS/ES/CS/SLBT, when specified by AI instruction in the specified location
10. CN stands for China
11. WD stands for Western Digital®
12. Follow factory ESD procedure.
13. Warning: Digital or paper copies of this document must not be relied upon unless document control procedure is followed.

5 S5E Signals

Table 4: S5E Signal Descriptions (in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
0	Power and ground	VDDIO_2	1.23V/ 1.8V					NAND I/F IO suuply
		VDDIO_1						External I/F supply
		PCIe_ AVDD_H	1.23V/ 1.8V					PCIe voltage supply
		AVDD1X_ PLL						PLL voltage supply
		VQPS	1.8V					Fuse burning supply (ONLY). Otherwise, connect to VSS
		PCIe_ VDD	0.835V/ 0.9V					PCIe digital supply
		V_{DD_PLL}						PLL digital supply
		V_{DD}						Core digital supply
		V_{CC}	2.5V					Power supply to the NAND Flash array (not connected to the controller)
		V_{PP}	12V					NAND Flash supply (not connected to the controller)
		V_{SS}	0V					Global chip ground
		VSS_R	0V					Shield contact resistance measurement. When not used for measurement, pins must always be treated as VSS
1	PCIe	PCIe_ CLKREQ_ N[1]	V_{DDIO}_1	In + Out0	In/In + Out0	In/In + Out0	Float	PCIe clock request, active low
2		PCIe_ TX0_P	PCIe_ AVDD_ H					Differential TX lane 0
		PCIe_ TX0_N	PCIe_ AVDD_ H					
		PCIe_ RX0_P	PCIe_ AVDD_ H					Differential RX lane 0
		PCIe_ RX0_N	PCIe_ AVDD_ H					

Table continues on next page

Table 4: S5E Signal Descriptions (cont'd)(in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
2 cont	PCIe cont'd	PCIE_REFCLK_P	PCIe_AVDD_H					Differential PCIe PHY reference clock
		PCIE_REFCLK_N	PCIe_AVDD_H					
		PCI_RESREF	PCIe_AVDD_H					Reference pin. Requires 200Ω resistor in parallel to 10pF
1	Clock and Reset	CLK_IN	V_{DDIO}_1	In	In	In	In	24 MHz reference clock
		RESETN	V_{DDIO}_1	In	In	In	In	Power-On Reset and Global Reset, active low
3	Voltage source[5]	ANI0_VREF[7]		Disabled	Enabled	Enabled	Disabled /Enabled (Note 6)	ANI0 voltage reference source. Could be an output (internal V_{REF}) or input (external V_{REF}, generated from on-board resistor ladder)
		ANI1_VREF[7]		Disabled	Enabled	Enabled	Disabled /Enabled (Note 6)	ANI1 voltage reference source. Could be an output (internal V_{REF}) or input (external V_{REF}, generated from on-board resistor ladder)
	Cal	ZQ_0[7]		Float	Float	Float	Float	ANI0 controller and NAND_ZQ calibration. Use an on-board 300Ω pull-down.
		ZQ_1[7]		Float	Float	Float	Float	ANI1 controller and NAND_ZQ calibration. Use an on-board 300Ω pull-down.
NA	NAND	WP_N	V_{DDIO}_2	NA	NA	NA	NA	Write_Protect_N—Pin connected to NAND only
1	SW	DROOP_N	V_{DDIO}_1	Float	Float	Float	Float	DROOP_N—In functional mode, can be used as droop indication to SW.
	EXT (all in HW_BYPASS mode)	EXT_D7\SPF_N	V_{DDIO}_1	Float	In	In	In/Out	EXT_D7 in HW_BYPASS mode. Host channel 7th-bit, bidirectional port for transferring address, command, and data to and from the device SPF_N – Sudden Power Fail notification

Table continues on next page

Table 4: S5E Signal Descriptions (cont'd)(in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
1 cont	EXT cont'd	EXT_D6\ BOOT3	V_{DDIO}_1	In + PD	Float	Float	In/Out	EXT_D6 in HW_BYPASS mode. Host channel 6th-bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap3—Input enabled by default—for SW read
		EXT_D5\ SPINAND_MOSI\ SPI_MOSI\ SWD_UID1	V_{DDIO}_1	Float	Float	Float	In/Out	EXT_D5 in HW_BYPASS mode. Host channel 5th-bit, bidirectional port for transferring address, command, and data to and from the device SPINAND_MOSI – SPI_MOSI pin in SPINAND mode SPI_MOSI – SPI_MOSI pin in SPI mode SWD_UID1 - Proprietary GPIO Unique ID1
		EXT_D4\ SPI_CS	V_{DDIO}_1	Float	Float	Float	In/Out	EXT_D4 in HW_BYPASS mode. Host channel 4th-bit, bidirectional port for transferring address, command, and data to and from the device SPI_CS – SPI Chip Select
		EXT_D3\ SPINAND_MISO\ SPI_MISO\ SWD_UID0	V_{DDIO}_1	In	Float	Float	In/Out	EXT_D3 in HW_BYPASS mode. Host channel 3rd-bit, bidirectional port for transferring address, command, and data to and from the device SPINAND_MISO – SPI_MISO pin in SPI mode SPI_MISO – SPI_MISO pin in SPINAND mode SWD_UID0 - Proprietary GPIO Unique ID0

Table continues on next page

Table 4: S5E Signal Descriptions (cont'd)(in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
1 cont	EXT cont'd	EXT_D2\ BOOT2\ SPINAND_SCLK\ SPI_SCLK	V_{DDIO}_1	In	Float	Float	In/Out	EXT_D2 in HW_BYPASS mode. Host channel 2nd-bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap2 – Input enabled by default- for SW read. SPINAND_SCLK – SPI_SCLK pin in SPINAND mode SPI_SCLK – SPI_SCLK pin in SPI mode
		EXT_ D1\ BOOT1	V_{DDIO}_1	In + PD	In	In	In/Out	EXT_D1 in HW_BYPASS mode. Host channel 1st-bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap1—Input enabled by default—for SW read GPIO – GPIO used as proprietary FW indication
		EXT_D0\ BOOT0	V_{DDIO}_1	In + PU	Float	Float	In/Out	EXT_D0 in HW_BYPASS mode. Host channel 0th-bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap0—Input enabled by default—for SW read
		EXT_DQS\ BCM_N	V_{DDIO}_1	In + PU	Float	Float	Float/ In\Out[8]	mode. The data strobe signal that indicates the data valid window for the source synchronous-data interface. Complementary signal is not in use. Pad disabled in bypass SDR mode BCM_N (Backward Compatibility Mode) bootstrap

Table continues on next page

Table 4: S5E Signal Descriptions (cont'd)(in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
1 cont	EXT cont'd	EXT_NCE \ PERSTN	V_{DDIO}_1	In	In	In	In + PU	EXT_NCE in HW_BYPASS mode. The Chip Enable signal selects the target. When CEn is high and the target is in normal ready mode, the target goes into an IDLE mode. When CEn is low, the target is selected. PERSTN—In functional mode, PCIe-side reset event—handled by SW.
		EXT_RNB \JTAG_ TDO	V_{DDIO}_1	Float	Float	Float	Out + PU	EXT_RnB in HW_BYPASS mode. Ready/Busy signal indicates the device status when legacy cmds (read, program, erase, reset) are executed. When low, the signal indicates that one or more operations are in progress. JTAG_TDO – JTAG Test Data Out bit
		EXT_NRE \ JTAG_TM S	V_{DDIO}_1	In + PU	In + PU	In + PU	In + PU	EXT_NRE in HW_BYPASS mode. Read Enable signal enables data output JTAG_TMS – JTAG Test Mode Select bit
		EXT_ALE \ JTAG_SE L	V_{DDIO}_1	In + PD	In + PD	In + PD	In + PD	EXT_ALE in HW_BYPASS mode. The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data) JTAG_SEL – JTAG Select bit
		EXT_CLE \ JTAG_TDI	V_{DDIO}_1	In + PU	In + PU	In + PU	In + PU	EXT_CLE in HW_BYPASS mode. The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). JTAG_TDI – JTAG Test Data In bit

Table continues on next page

Table 4: S5E Signal Descriptions (cont'd)(in pin mode)

Pad Type	I/F	Pin Name	Domain	Value at Resetn-0	Value at L.P. Boot	Value at Normal Boot	Value at Bypass	Description/Notes
1 cont	EXT cont'd	EXT_NWE \JTAG_TCK	V_{DDIO}_1	In + PU	In + PU	In + PU	In + PU	EXT_NWE in HW_BYPASS mode. The Write Enable signal controls input data latching in the asynchronous data interface. Data, commands, and addresses are latched on the rising edge of WE#. JTAG_TCK – JTAG Clock bit
	JTAG	TRSTN	V_{DDIO}_1	In + PD	In + PD	In + PD	In + PD	JTAG_TRSTN – JTAG Test Resetn.

Note 1. While in IN mode, line is pulled up by external on-board pull-up.

2. PU = Pull-up, PD = Pull-down.
3. Pin states shown in the LP boot and Normal boot columns reflect the state at the end of the boot; i.e., this state also corresponds to LP- and Normal-mode operation.
4. Device LP or Normal boot is scenario dependent.
5. When internal V_{REF} is disabled, the pad is floating.
6. V_{REF} is disabled in bypass SDR mode and enabled in bypass DDR mode.
7. Pad configuration is referring to the controller only (i.e., not to NAND ZQ or V_{REF} pads).
8. EXT_DQS is "Float" in bypass SDR mode and "In/Out" in bypass DDR mode.

6 Electrical Characteristics

6.1 AC Electrical Characteristic

For AC Digital-Pin Characteristics please reference the package data sheet.

Table 5: AC Analog-Pin Characteristics

Parameter	Min (µs)	Max (µs)	Notes
tVREF	—	10	Ramp time for ANIx_VREF with no external on-board load

Note 1. V_{REF} refers to rise time: 0–100% of the internal ANIx_VREF generators.

6.2 DC Electrical Characteristics

Table 6: DC Digital-Pin Characteristics

Description	Symbol	Min	Typ	Max	Units
Input capacitance (controller's pad only)	C_{IN}	—	—	3	pF
Input leakage current at Vi = 1.8V or 0V	I_{IN}	—	—	4	µA
High-level output current at V_{OH} (min)	I_{OH}—Type 1.1	6.3	12.3	20.9	mA
High-level output current at V_{OH} (min)	I_{OH}—Type 1.2	4.1	8.1	13.7	mA
Low-level output current at V_{OL} (max)	I_{OL}—Type 1.1	8	14.9	24	mA
Low-level output current at V_{OL} (max)	I_{OL}—Type 1.2	5	9.4	15.2	mA
Pull-down resistor	R_{PD}	42.7	72.8	140.3	KΩ
Pull-up resistor	R_{PU}	49.1	79.5	148.3	KΩ
Input high voltage	V_{IH}	0.7	—	1.0	V
Input low voltage	V_{IL}	-0.3	—	0.3	V
Output high voltage	V_{OH}	0.96	—	—	V
Output low voltage	V_{OL}	—	—	0.24	V

Table 7: DC Internal-Interface-Pin Characteristics

Description	Symbol	Min	Typ	Max	Units
Pull-down resistor	R_{PD}	0.75	—	2	KΩ
Pull-up resistor	R_{PU}	0.75	—	2	KΩ

Table 8: DC V_{REF}-Pin and ZQ-Pin Characteristics

Description	Symbol	Min	Typ	Max	Units
Input leakage current at Vi = 0.9V or 0V (at MCP level)	ANIx_ VREF_Iin	—	—	± 20	µA
Input leakage current at Vi = 1.8V or 0V	ZQ_C_Iin	—	—	± 20	µA

7 S5E Device Timing

7.1 Power-State Transitions

Table 9: S5E VFW Power-State Transition Requirements

Beginning State	Target State	Min	Max	Units
Off	LP mode	0	110	ms
Off	Normal mode	0	80	ms
LP mode	Normal mode	0	8	ms
Normal mode	Idle CG	0	100	µs
Normal mode	Idle PG	0	500	µs
Normal mode	Deep PG	0	1000	µs
Idle clock gated (CG)	Normal mode	0	60	µs
Idle power gated (PG)	Normal mode	0	500	µs
Deep PG	Normal mode	0	Note 1	

Note 1. Deep PG to Normal latency is primarily dependent on PCIe host enumeration time.

8 Power

8.1 Idle Power

Table 10: Idle Power

State	Temperature °C	V_{DD} [mA]	V_{CCQ} [mA][1]	V_{CC} [mA]	V_{PP} [mA]
Idle clock gated	85	60	1.2	Vendor specific	Vendor specific
	25	10	0.6		
	–15	10	0.6		
Idle power gated	85	13	0.4		
	25	2	0.2		
	–15	1.5	0.2		
Idle deep power gated	85	13	0.52		
	25	2	0.32		
	–15	1.5	0.32		

Note 1. I_{NAND} = worst case of single NAND V_{DDIO} current consumption.

8.2 Average Power

Table 11: Active Average Power: Normal Mode

Temp	Op Mode	State	2 Die			8 Die		
			I_{DD} [mA]	I_{CCQ} [mA]	I_{CC} [mA]	I_{DD} [mA]	I_{CCQ} [mA]	I_{CC} [mA]
25°C	MLC/TLC	Program	80	37	74	121	47	297
		Read	153	47	127	152	46	125
	SLC	Program	113	45	116	120	46	140
		Read	142	46	109	150	46	118

8.3 Peak Power

Peak power consumption varies with each use case. Noted current limits in Tables 12 and 13 reflect peak power measured across 1µs, 5µs, and 20µs. The limits in each table reflect worst-case corner at 85°C.

Table 12: Worst-Case Average Maximum (guaranteed not-to-exceed) I_{DD} and I_{DDIO} Currents

State	CLK_IN frequency	V_{DD} [mA]	V_{CCQ} [mA]*
Inrush[1] (ramp rate)	Don't care	5	1
Power up		60	1.5
Reset	1 MHz	75	1.5
Bypass entry		100	1.5
Bypass[2, 3]		60	2
Reset	24 MHz	105	1.5
Bypass entry		110	1.5
Bypass[2, 3]		70	2
Pads test mode (CLK_IN is off)		25	1.5
Low power Boot		205	34
Normal mode (without PCIe)		560	72
Normal mode (with PCIe in ext. loop-back)		700	72

Note 1. Inrush current is measured without decoupling capacitors, with fastest ramp time at 85°C.
2. Bypass-mode current assumes CLK_IN keeps toggling at 1MHz/24MHz.
3. Bypass assumes WR, SDR, 17MHz. RD path may consume more power, depending on tester load.

Table 13: Power Budget

Configuration (die/MCP)	Die in Parallel	PB	NAND PPM	Program Cache	Read Cache	BG I/O	1µs	5µs	20µs
2	2	NRP	Dis	En	En	N/A	N/A	N/A	N/A
	2	**A (max)**	Dis	En	En	N/A	387	284	224
4	4	PB2 (max)	Dis	En	En	N/A	688	403	309
8	2	NRP	Dis	Dis	Dis	BG I/O	N/A	N/A	N/A
	2	A	Dis	Dis	Dis	BG I/O	N/A	N/A	N/A
	4	B	Dis	Dis	Dis	BG I/O	N/A	N/A	N/A
	8	C	En	Dis	Dis	N/A	N/A	N/A	N/A
	8	D (max)	Dis	En	Dis	N/A	987	598	458
16	16	S2 (max)	Dis	En	Dis	N/A	919	639	508

Note 1. The maximum power budget for each configuration is highlighted.

2. BG I/O indicates that other unselected die are not receiving Program commands. Use the Program Cache expected-results formula from the product spec.
3. This table assumes FW10 PB use. Updates could be planned in subsequent FW releases.
4. The default PB is NRP for Normal mode.
5. Max = actual maximum POR PB planned for use at the system level.

9 Performance

Table 14: Typical Performance

Power Mode Scenario:		MLC/TLC Performance Targets			SLC Performance Targets		
		Sequential Program throughput	Sequential Read throughput	4KB Read latency, active (ASPM = dis)	Sequential Program throughput	Sequential Read throughput	4KB Read latency, active (ASPM = dis)
		MBps	MBps	µs	MBps	MBps	µs
2 Die	Low power	N/A	46	183	N/A	48	150
	Normal PB NPR	204	849	N/A	804	850	N/A
4 Die	Low power	N/A	46	184	N/A	48	150
	Normal PB NPR	207	887	N/A	902	889	N/A
8 Die	Low power	N/A	46	184	N/A	48	150
	Normal PB NPR	209	886	74	892	888	56
	Normal PB A	211	886	73	892	888	54
	Normal PB B	420	887	73	899	889	54
	Normal PB C	631	887	73	901	890	54
	Normal PB D	773	895	72	908	898	54
16 Die	Low power	N/A	46	183	N/A	48	150
	Normal PB NPR	209	883	74	858	886	56

Table 15: Block Erase Time

Operation	Typ	Max
Block Erase time (single block)	10ms	15ms

10 Revision History

Table 16: History

Status	Rev. #	Date	Changes
Preview	0.1	7/1/20	Initial release
Preview	0.2	8/13/20	• Table 1, "3D S5E Gen5 X3 512Gb 2-Plane Features," on page 1: Added package information on page 2 • Figure 2, "110-Ball BGA Assignments—Top View, Pads Down," on page 5: Removed draft watermark • Figure 3, "Package Outline Diagram: 1-Die, 2-Die, 4-Die, 5-Die, and 8-Die Stacks," on page 6: Added figure • Figure 4, "Package Outline Diagram: 9-Die and 16-Die Stacks," on page 7: Added figure
Production	1.0	7/22/21	• Updated document, replacing TBDs throughout with the appropriate values • Removed former Table 3 and referred readers to the B5 X3 512Gb 2-Plane package data sheet • Table 9, "S5E VFW Power-State Transition Requirements," on page 24: Removed former note 1 and moved note 2 up • Table 10, "Idle Power," on page 24: Removed former note 2 • Table 12, "Worst-Case Average Maximum (guaranteed not-to-exceed) IDD and IDDIO Currents," on page 25: Added note 3 cross-references to both Bypass state entries • Updated document to Production status
Production	1.1	8/12/21	• Table 1, "3D S5E Gen5 X3 512Gb 2-Plane Features," on page 1: Corrected TLC typical Page Program to 1005µs
Production	1.2	9/10/21	• "Marketing Part Numbers" on page 0: —Added note and cross references to Mk2 content • Table 3.1, "Standard Packaging," on page 6: Added new subsections and 3.1.2 content: —"3.1.1 Standard Package Outline Drawings" on page 6 —"3.2 Mk2 Packaging" on page 8 and text —"Table 2: Mk2 Package Numbers and Configuration: SDSS SKUs" on page 8
Production	1.3	12/15/21	• Table 2, "Mk2 Package Numbers and Configuration: SDSS SKUs," on page 8: Added ten new SKUs
Production	1.4	2/7/22	• Table 1, "3D S5E Gen5 X3 512Gb 2-Plane Features," on page 1: Updated Modes section, defining array dependence • Table 2, "Mk2 Package Numbers and Configuration: SDSS SKUs," on page 8: Updated table and added two new SKUs for Thin-Micro devices; highlighted SKU numbers nearing EOL; added note with SKU# EOL timing **Change Order:** Customer's request • Table 2: —Added APN column • Table 3, "Mk2 Package Numbers and Configuration: SDSM SKUs," on page 8: Inserted new table with SKUs for SDSM devices and provided column for APNs that are currently TBD
Rev. 1.4 continues on next page			

Table 16: History

Status	Rev. #	Date	Changes
Production	1.4	2/7/22	**Change Order:** Customer's request • Added sections: —"3.2 Mk2 Packaging" on page 8 —"3.2.1 MK2 LGA Pad Assignments" on page 9 Inserted Mk2-specific content from former POD book • "Table of Contents" on page i: Added for improved navigation with the increase in document size and similarity of new content to pre-existing content • Updated company headquarters address on page 27
Production	1.5	6/23/22	• Table 2, "Mk2 Package Numbers and Configuration: SDSS SKUs," on page 8, **and** Table 3, "Mk2 Package Numbers and Configuration: SDSM SKUs," on page 8: Updated part numbers and descriptions; in Table 3, added a new column for SKU Sub-Y part numbers

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