S6E + BiCS FLASH™ generation 8
iTLC3 & iTLC5 with Mk2 Package
Simplified Technical Data Sheet

Rev.0.1

2023/9/7

KIOXIA Corporation

Description

These devices are S6E MCP NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) of 128GByte/256GByte/512GByte/1TByte/2TByte. These devices are composed of BiCS FLASH™ generation 8 1Tbit TLC 4plane Die and these TLC(3bits per cell) devices are supposed to be operated with TLC mode. Here it is allowed to use these devices with SLC(1bit per cell)/TLC mixed condition and the density and capacity of them is depend on the ratio of usage between SLC and TLC in a device. Then the density and capacity is defined by the size based on logical address area with TLC 100% usage mode in this document.

A KIOXIA S6E MCP NAND device includes:

- A S6E Controller
- BiCS FLASH™ generation 8 1Tbit TLC 4plane raw NAND dies
- One lane of PCIe interface

Note: The Memory density to the number of DP is rounded down to the nearest integer in this document.

■ BiCS FLASH™ generation 8 1Tbit TLC 4plane die

128 GBytes indicates the rounding result of calculation of (1Tbit/8bits)*1DP.

256 GBytes indicates the rounding result of calculation of (1Tbit/8bits)*2DP.

512 GBytes indicates the rounding result of calculation of (1Tbit/8bits)*4DP.

1024 GBytes indicates the rounding result of calculation of (1Tbit/8bits)*8DP.

2024 GBytes indicates the rounding result of calculation of (1Tbit/8bits)*16DP.

*DP is short for Die stacked Package. And the notation of “nDP” means # of die stack.

■ Mk2 Package

- Micro Package :
  - Type 1 : 13.3 mm x 9.0 mm x 0.75 mm
  - Type 2 : 13.3 mm x 9.0 mm x 0.9 mm
- Mini Package : 13.3 mm x 11.0 mm x 1.3 mm

Features

From Table 1 to Table 2 show these device features.

Table 1 Part Number (iTLC3 & iTLC5)

Part Number for MP (15digit)	Part Number for Qual (16digit)	NAND Die	Trim	DP	Package Type	Wafer Fab	Substrate Type	Assembly Fab
THGJY9T0C18LFAS	THGJY9T0C18LFAS0	BiCS FLASH™ generation 8 1Tbit TLC 4plane	iTLC3	1	Micro Package Type 1	YOK	X	PTI
	THGJY9T0C18LFASA						Y	AMK
	THGJY9T0C18LFAS1		iTLC5				X	PTI
	THGJY9T0C18LFASB						Y	AMK
THGJY9T1C28LFAS	THGJY9T1C28LFAS0		iTLC3	2			X	PTI
	THGJY9T1C28LFASA						Y	AMK
	THGJY9T1C28LFAS1		iTLC5				X	PTI
	THGJY9T1C28LFASB						Y	AMK
THGJY9T2C48LFAS	THGJY9T2C48LFAS0		iTLC3	4			X	PTI
	THGJY9T2C48LFASA						Y	AMK
	THGJY9T2C48LFAS1		iTLC5				X	PTI
	THGJY9T2C48LFASB						Y	AMK
THGJY9T3C88LFAN	THGJY9T3C88LFAN0		iTLC3	8	Micro Package Type 2		X	PTI
	THGJY9T3C88LFANA						Y	**TBD**
	THGJY9T3C88LFAN1		iTLC5				X	PTI
	THGJY9T3C88LFANB						Y	**TBD**
THGJY9T4CB8LFAP	THGJY9T4CB8LFAPA		iTLC3	16	Mini Package		Y	YOK
	THGJY9T4CB8LFAPB		iTLC5				Y	YOK

[Note] KIOXIA will use YOK assembly fab for Proto and controller corner samples.

Table 2 Organization

Parameter	Value
Page size	18,336 Bytes
Number of Pages	3,270
Block size	59,958,720Bytes
Number of Blocks	2,748
Number of Planes	4

Pin Assign (Top View)

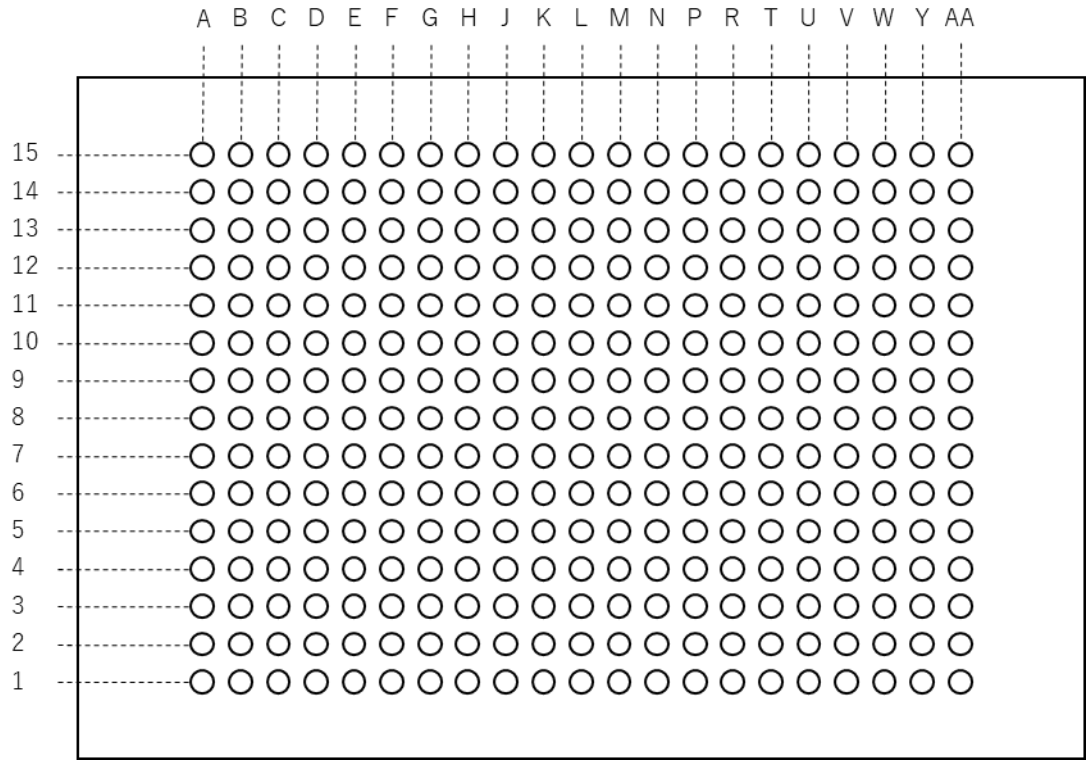

Figure 1 Pin Assign (Top View)

Pin Names

Table 3 Pin names and description

Pin Location	Signal Name	Type	Description
P9, P10	PCIE_AVDD_H	Power	PCIe voltage supply
G5, G11, H5, H11, P5, P11, R5, R11	VDDIO_1	Power	External interface supply
G4, G12, H4, H12, K4, K12, L4, L12, M4, M12, P4, P12, R4, R12	VDDIO_2	Power	NAND IF IO Supply
N6	AVDD12_PLL	Power	PLL voltage supply
H6	VQPS	Power	Fuse burning supply. VQPS should be connected to GND.
P7, R7, R9	PCIE_VDD	Power	PCIE digital supply
M6	VDD_PLL	Power	PLL digital supply
J7, J9, K7, K9, M7, M9, N7, N9	VDD	Power	Core digital supply
E11	VPP	Power	NAND supply
E4, E12, F4, F12, T4, T12, U4, U12	VCC	Power	Power supply to the NAND array

Pin Location	Signal Name	Type	Description
A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, C1, C2, C3, C4, C12, C13, C14, C15, D1, D2, D3, D13, D14, D15, E1, E2, E3, E13, E14, E15, F1, F2, F3, F5, F11, F13, F14, F15, G1, G2, G3, G13, G14, G15, H1, H2, H3, H7, H8, H13, H14, H15, J1, J2, J3, J4, J5, J8, J11, J12, J13, J14, J15, K1, K2, K3, K8, K13, K14, K15, L1, L2, L3, L7, L8, L9, L13, L14, L15, M1, M2, M3, M8, M13, M14, M15, N1, N2, N3, N5, N8, N12, N13, N14, N15, P1, P2, P3, P8, P13, P14, P15, R1, R2, R3, R6, R8, R10, R13, R14, R15, T1, T2, T3, T5, T7, T9, T11, T13, T14, T15, U1, U2, U3, U5, U7, U9, U11, U13, U14, U15, V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y12, Y13, Y14, Y15, AA1, AA2, AA3, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA11, AA12, AA13, AA14, AA15	VSS	GND	Global chip ground
P6	PCIE_CLKREQ_L	I/O	PCIe clock request
U10	PCIE_TX0_P		Differential Tx lane 0
T10	PCIE_TX0_N		
U8	PCIE_RX0_P		Differential Rx lane 0
T8	PCIE_RX0_N		
T6	PCIE_REFCLK_P		Differential PCIe PHY reference clock

Pin Location	Signal Name	Type	Description
U6	PCIE_REFCLK_N		
N10	PCIE_ TSTREF		Test pin for internal use
N11	CLK_IN	I	24MHz Reference clock
J6	RESET_L	I	Power on reset and Global reset
K5	ZQ_1	Calibration Pin	ANI1 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
M11	ZQ_0	Calibration Pin	ANI0 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
E5	WP_L	I	Write protect. Connected to NAND
N4	DROOP_L		Proprietary use
G10	EXT_D7 / SPF_L	I/O	EXT_D7: Data for HW Bypass mode SPF_L: Sudden Power Fail notification
F9	EXT_D6 / BOOT3	I/O	EXT_D6: Data for HW Bypass mode Bootstrap3: Input enabled by default- for SW read.
E9	EXT_D5 / SPINAND_MOSI / SPI_MOSI / SWD_UID1	I/O	EXT_D5: Data for HW Bypass mode SPINAND_MOSI: SPI_MOSI pin in SPINAND mode SPI_MOSI: SPI_MOSI pin in SPI mode SWD_UID1: Proprietary GPIO Unique ID1
G9	EXT_D4 / SPI_CS	I/O	EXT_D4: Data for HW Bypass mode SPI_CS: SPI Chip Select
E8	EXT_D3 / SPINAND_MISO / SPI_MISO / SWD_UID0	I/O	EXT_D3: Data for HW Bypass mode SPINAND_MOSI: SPI_MISO pin in SPINAND mode SPI_MISO: SPI_MISO pin in SPI mode SWD_UID0: Proprietary GPIO Unique ID0
F8	EXT_D2 / BOOT2 / SPINAND_SCLK / SPI_SCLK	I/O	EXT_D2: Data for HW Bypass mode Bootstrap2: Input enabled by default for SW read SPINAND_SCLK: SPI_SCLK pin in SPINAND mode SPI_SCLK: SPI_SCLK pin in SPI mode
H9	EXT_D1 / BOOT1	I/O	EXT_D1: Data for HW Bypass mode Bootstrap1: Input enabled by default for SW read
G8	EXT_D0 / BOOT0	I/O	EXT_D0: Data for HW Bypass mode Bootstrap0: Input enabled by default for SW read
E10	EXT_DQS / BCM	I/O	EXT_DQS in HW_BYPASS (DDR) mode. BCM (Backward Compatibility Mode) bootstrap
F10	EXT_NCE / PERST_L	I	EXT_NCE: NCE for HW Bypass mode PERST_L: In functional mode, PCIe side reset event. SW handled.

Pin Location	Signal Name	Type	Description
G6	EXT_RNB / JTAG_TDO	O	EXT_RNB: RnB for HW Bypass mode JTAG_TDO: JTAG Test Data Output bit
E6	EXT_NRE / JTAG_TMS	I	EXT_NRE: NRE for HW Bypass mode JTAG_TMS: JTAG Test Mode Select bit
E7	EXT_ALE / JTAG_SEL	I	EXT_ALE: ALE for HW Bypass mode JTAG_SEL: JTAG Select bit
G7	EXT_CLE / JTAG_TDI	I	EXT_CLE: CLE for HW Bypass mode JTAG_TDI: JTAG Test Data In bit
F6	EXT_NWE / JTAG_TCK	I	EXT_NWE: NWE for HW Bypass mode JTAG_TCK: JTAG Clock bit
F7	JTAG_TRSTN	I	JTAG Test Reset
C5, C6, C7, C8, C9, C10, C11, D4, D5, D6, D7, D8, D9, D10, D11, D12, H10, J10, K6, K10, K11, L5, L6, L10, L11, M5, M10, Y11	NC	-	Non Connect (Floating individually)

Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VDD	Controller digital logic power supply voltage	0 to 0.96	V
VCCQ_ANI(*3)(*4)	ANI I/O voltage	0 to 1.26/1.3	V
VCCQ_IO	Controller I/O voltage	0 to 1.32	V
VQPS (*1)	Fuse burn supply voltage	0 to 1.85	V
VCC	NAND power supply voltage	-0.6 to 4.6	V
VPP (*2)	NAND power supply voltage	0 to 16	V
V_{IN}	IO pins input voltage	-0.3 to 1.98	V
V_{IN} (VCCQ_ANI=1.23V)	Input voltage for Internal raw NAND (WP_L pins)	-0.2 to 1.5	V

(*1) VQPS shall be tied to 1.8V only for fuses burn. For all other uses pin shall be connected to GND.

(*2) S6E + BiCS FLASH™ generation 8 MCP device doesn't support VPP function.

(*3) Platforms that share VccQ_IO & VccQ_ANI supply,may use the lower rating of the two supplies.

(*4) 1.3V is allowed only with BCM operation.

Temperature Conditions

Table 5 Temperature Conditions

Symbol	Rating	Value	Unit
T_{SOLDER} (10s)	Soldering Temperature	240	°C
T_{STR}	Storage Temperature	-15 to 85	°C
T_{OPR}	Operating case Temperature	-15 to 85 (*1)	°C

(*1) Evaluating potential spec extension to -25 ~ 100C.

Recommended Operating Conditions

Table 6 Operation Mode

Operation Mode	VDD [V]	VccQ_IO [V]	VccQ_ANI [V]	VCC [V]	BCM	PCIe Gen	ANI Frequency [MHz]
1	0.835	1.2	1.2	2.5	"0"	5	1200(RD/WR)/1400(RD)
2	0.835	1.2	1.23	2.5	"1"	4	600

[Note] BCM(EXT_DQS) pin is used as a bootstrap for indicating IO supplies voltage for S6E controller.

Table 7 Recommended Operationg Conditions

Symbol	Min	Typ	Max	Unit	Notes
VCCQ_IO	1.14	1.23	1.3	V	VCCQ_IO operation mode
VCCQ_ANI	1.14	1.2	1.26	V	VccQ_ANI operation mode for >600MHz
	1.14	1.23	1.3	V	VccQ_ANI operation mode for 600MHz
VQPS(*2)	Connected to GND				Fuse burn supply.
VDD	0.785	0.835	0.96	V	Low VDD operation mode
VCC	2.35	N/A	2.75	V	VCC rail is supplying NAND dies only
VPP (*1)	11	12	13	V	VPP rail is supplying NAND dies only

(*1) S6E + BiCS FLASH™ generation 8 MCP device doesn't support VPP function.

(*2) VQPS shall be tied to 1.9V only for fuses burn. During this phase, supply shall be on for no more than 200mS. For all other pin shall be connected to VSS.

Package Dimensions

(1) P-WFLGA315-0914-0.50-001 (Micro Package 0.75mm Z-max)
(THGJY9T0C18LFAS / THGJY9T1C28LFAS / THGJY9T2C48LFAS)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

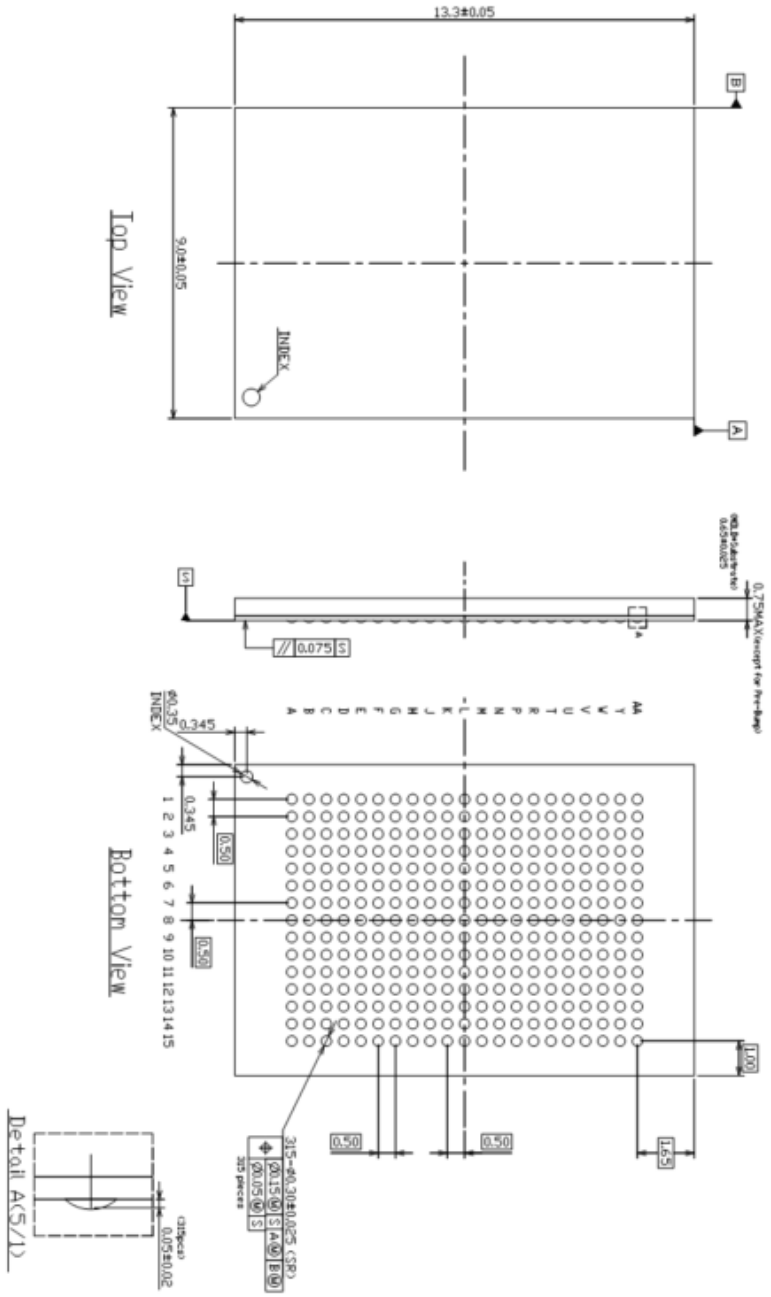

Figure 2 Package Dimension of P-WFLGA315-0914-0.50-001

(2) P-VFLGA315-0914-0.50-001 (Micro Package 0.9mm Z-max)
(THGJY9T3C88LFAN)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

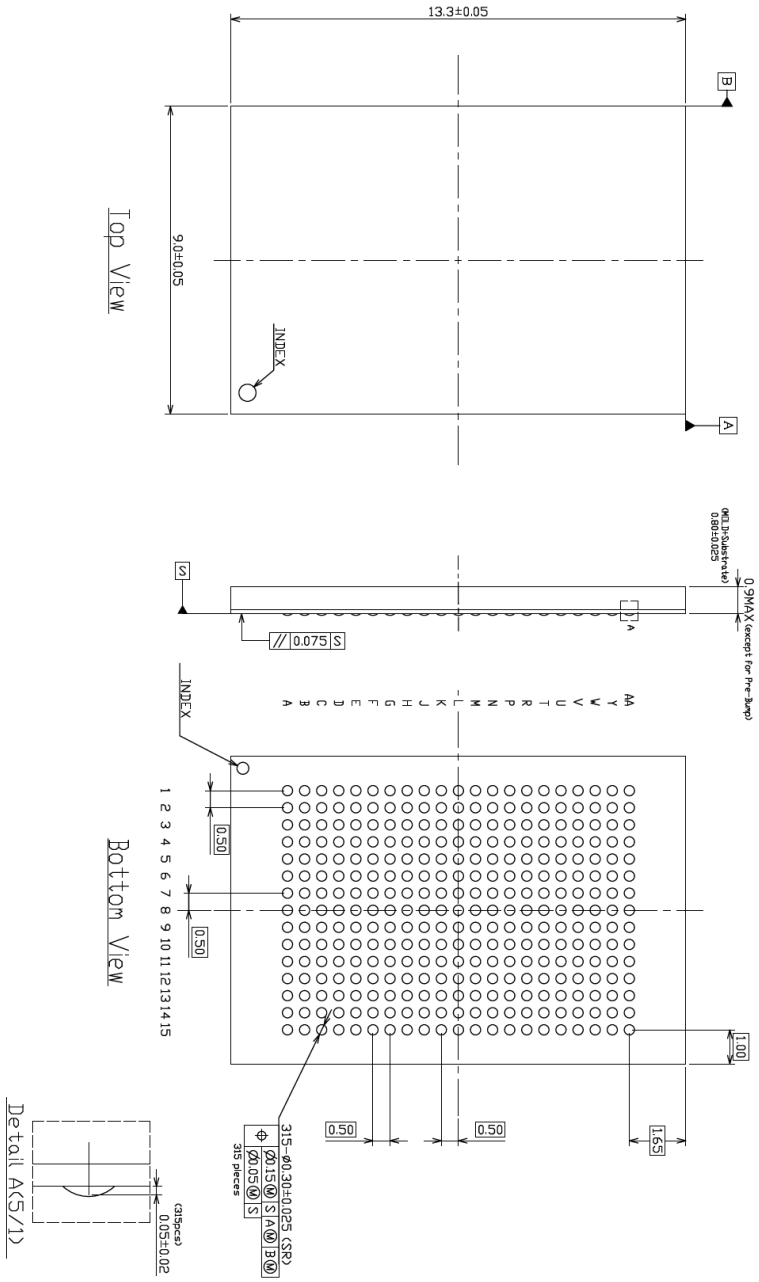

Figure 3 Package Dimension of P-VFLGA315-0914-0.50-001

(3) P-FLGA315-1114-0.50-001 (Mini Package 1.3mm Z-max)
(THGJY9T4CB8LFAP)

Note: Adopting a proper underfill is strongly required in order to meet system board level reliability.

Unit: mm

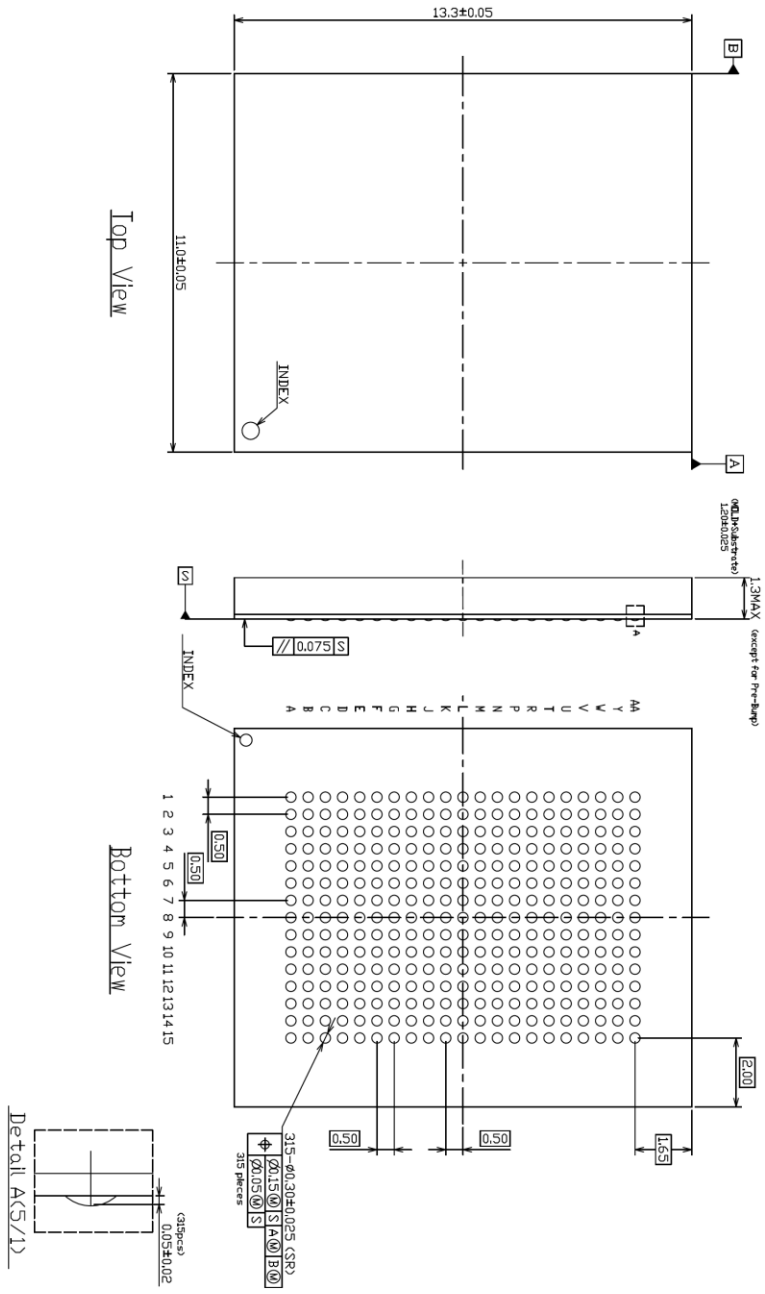

Figure 4 Package Dimension of P-FLGA315-1114-0.50-001

Table 8 Typical net weight of S6E + BiCS FLASH™ generation 8 MCP device

Kioxia's Part Number	Memory Die Type	Density	z-height	Typical Net weight
THGJY9T0C18LFAS	BiCS FLASH™ generation 8 1Tbit TLC 4plane	128GB	0.75mm	TBD
THGJY9T1C28LFAS		256GB	0.75mm	TBD
THGJY9T2C48LFAS		512GB	0.75mm	TBD
THGJY9T3C88LFAN		1TB	0.9mm	TBD
THGJY9T4CB8LFAP		2TB	1.3mm	TBD

Device Marking

Figure 5 shows the S6E + BiCS FLASH™ generation 8 MCP device marking image.

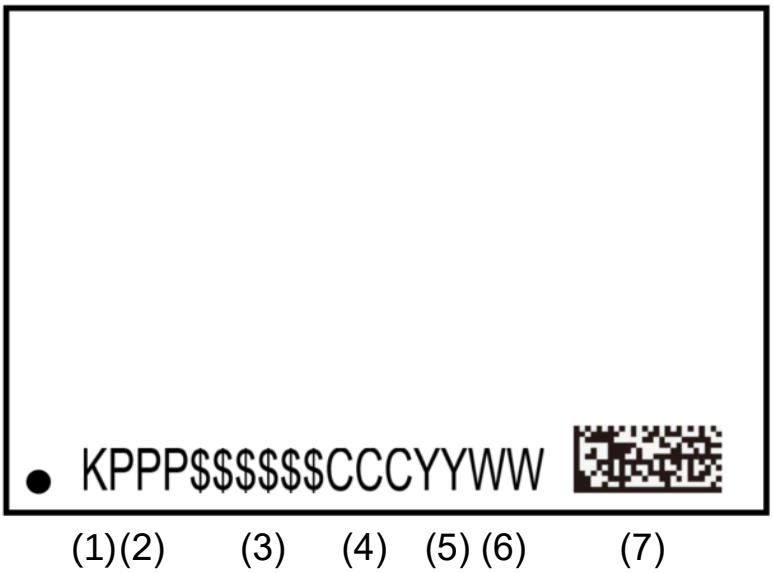

Figure5 S6E + BiCS FLASH™ generation 8 MCP Device marking image

Table 9 Device Marking Description

No.	Item	Comments
(1)	Vendor Name	1 digit; K: KIOXIA
(2)	Device Code	3 digits; Represents KIOXIA Part Number THGJY9T0C18LFAS (128GB/1DP) → 8A6 THGJY9T1C28LFAS (256GB/2DP) → 8A7 THGJY9T2C48LFAS (512GB/4DP) → 8A8 THGJY9T3C88LFAN (1024GB/8DP) → 8A9 THGJY9T4CB8LFAP (2024GB/16DP)→ 8B2
(3)	Key Number	6 digits; KIOXIA internal control code
(4)	Country of Assembly	1 digit; J (Japan) C (China) T (Taiwan)
(5)	Controller HW Version	2 digits; A0
(6)	Weekly Code	4 digits; YY : YY means lower two digits of the year. WW : WW is weekly code. (Weekly code complies with EIA standard)
(7)	2D Barcode	21 digits; It can be expressed with PPPDOMSSSSSEEEEEEEDRX by using mnemonic described in Table .

Table 10 2D Barcode Description

mnemonic	digit	Description	Format	Arbiter	Specification
PPP	21st -19th	Plant/Vender code	Alphanumeric	Apple	PPP means Plant/Vender code. The value is depending on the assembly site of samples. In case of YOK assembly the value shall be “DKG”. In case of PTI assembly the value shall be “FRK”. In case of AMK assembly the value shall be “FQ6”
DOM	18th -16th	Day of manufacture code	Alphanumeric	KIOXIA	DOM means Day of manufacture code. This is a three (3) character assigned by each Plant using the local date. The Day of Manufacturing is the count of days in Base 34 since January 1, 1970 through August 10, 2077. After this date the DOM characters will loop back to “000” and continue counting.
SSSSS (5S)	15th -11th	Sequential count code	Alphanumeric	KIOXIA	SSSSS means sequential count code. This is a five (5) character alphanumeric code Base34 counter assigned by each plant. The sequential count code ensures the module serial number (PPPDOMSSSSSEEEEEEE of 18digits code) is unique. The sequential count code has a dependency on the following segments of the module serial number: a) Day of Manufacturing code (DOM): All Sequential Counters reset to 00000 at the start of a new day, 00:00:00 AM local time. b) Engineering Configuration code (7E): Each 7E code has a separate unique SSSSS counter, per Plant Code (PPP). c) Plant Code (PPP): Each Plant Code will have a separate unique SSSSS counter, per 7E.Date
EEEEEEE (7E)	10th - 4th	Engineering configuration code	Alphanumeric	Apple	EEEEEEE means engineering configuration code. This is a seven (7) character alphanumeric code assigned by Apple. There is a one to one relationship between MPN and this code.
D	3rd	A delimiter to flag the end of serial number	“+”	-	The plus sign “+” is used as a delimiter to flag the end of the module serial number (PPPDOMSSSSSEEEEEEE of 18digits code).
R	2nd	Revision	Alphanumeric	Apple	R means Revision code. The value on the samples graded WS and ES shall be numeric in specification. It starts from “0” and it could be incremented according to the customer’s request. The increment rule is as follows. 0=>1=>2=>3 ・・・ The value on the samples graded CS, GS and MP shall be alphabet in specification. It starts from “A” and it could be incremented according to the customer’s request. The increment rule is as follows. A=>B=>C ・・・
X	1st	Checksum character	Alphanumeric	KIOXIA	X means Checksum Character. The algorithm is based on Modulo 34.

Revision History

Date	Rev.	Description
Sep.7th, 2023	0.1	Initial Release.

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