128/256/512/1024GB
E3NAND

128GB : HN3T0HT1DAX430
HN3T0HT1DAX434
256GB : HN3T1HT2DAX437
HN3T1HT2DAX435
512GB : HN3T2HT4DAX431
HN3T2HT4DAX436
1024GB : HN3T3HT8DAX431
2048GB : HN3T4HTGDAX433

Document Title
128 / 256 / 512 / 1024 / 2048GB E3NAND Specification

Revision History

Table1. Document Revision History

Revision No.	History	Draft Date
0.0	-. Draft version	Feb. 07. 2024
0.1	-. 16DP updated	Feb. 15. 2024
0.2	-. 2/4DP CQ, 8DP 0.75T updated	July. 29. 2024
0.3	-. 1DP CQ updated	Oct. 10. 2024
0.4	-. Added APN Table in page 8	Oct. 30. 2024

CONTENTS

1. Introduction

1.1. Goals and Objectives

This document communicates the specification for E3NAND

1.2. Key Features

■ Physical Interface

- PCIe Gen5

■ Memory Technology

- 1Tb 3bit per cell

■ E3NAND Organization

- 128GB : 1+1-stacks
- 256GB : 1+2-stacks
- 512GB : 1+4-stacks
- 1024GB : 1+8-stacks
- 2048GB : 1+16-stacks

■ Power Supply

- VDD for high VDD operational mode : TBD
- VDD for low VDD operational mode : TBD
- VCCQ for high VCCQ operational mode : TBD
- VCCQ for low VCCQ operational mode : TBD
- VCC : TBD

■ Net Weight

- 128GB : TBD [g]
- 256GB : TBD [g]
- 512GB : TBD [g]
- 1024GB : TBD [g]
- 2048GB : TBD [g]

■ Package

- 128/256/512/1024GB : LGA315 (09.0 x 13.3 X 0.75mm)
- 2048GB : LGA315 (11.0 x 13.3 X 0.9mm)

■ FW version

- TBD

■ E3NAND controller version

- S6E (TBD)

■ Operation Temp

- Case surface temperature (-25~100C)

1.3. Product List

1.3.1. Part number

Part Number	VDD	VDDIO	VCC	Organization	Density	B/E site
HN3T0HT1DAX430	TBD	TBD	TBD	1 + 1	128GB	CJ
HN3T0HT1DAX434	TBD	TBD	TBD	1 + 1	128GB	CQ
HN3T1HT2DAX437	TBD	TBD	TBD	1 + 2	256GB	CJ
HN3T1HT2DAX435	TBD	TBD	TBD	1 + 2	256GB	CQ
HN3T2HT4DAX431	TBD	TBD	TBD	1 + 4	512GB	CJ
HN3T2HT4DAX436	TBD	TBD	TBD	1 + 4	512GB	CQ
HN3T3HT8DAX431	TBD	TBD	TBD	1 + 8	1024GB	CJ
HN3T4HTGDAX433	TBD	TBD	TBD	1 + 16	2048GB	CJ

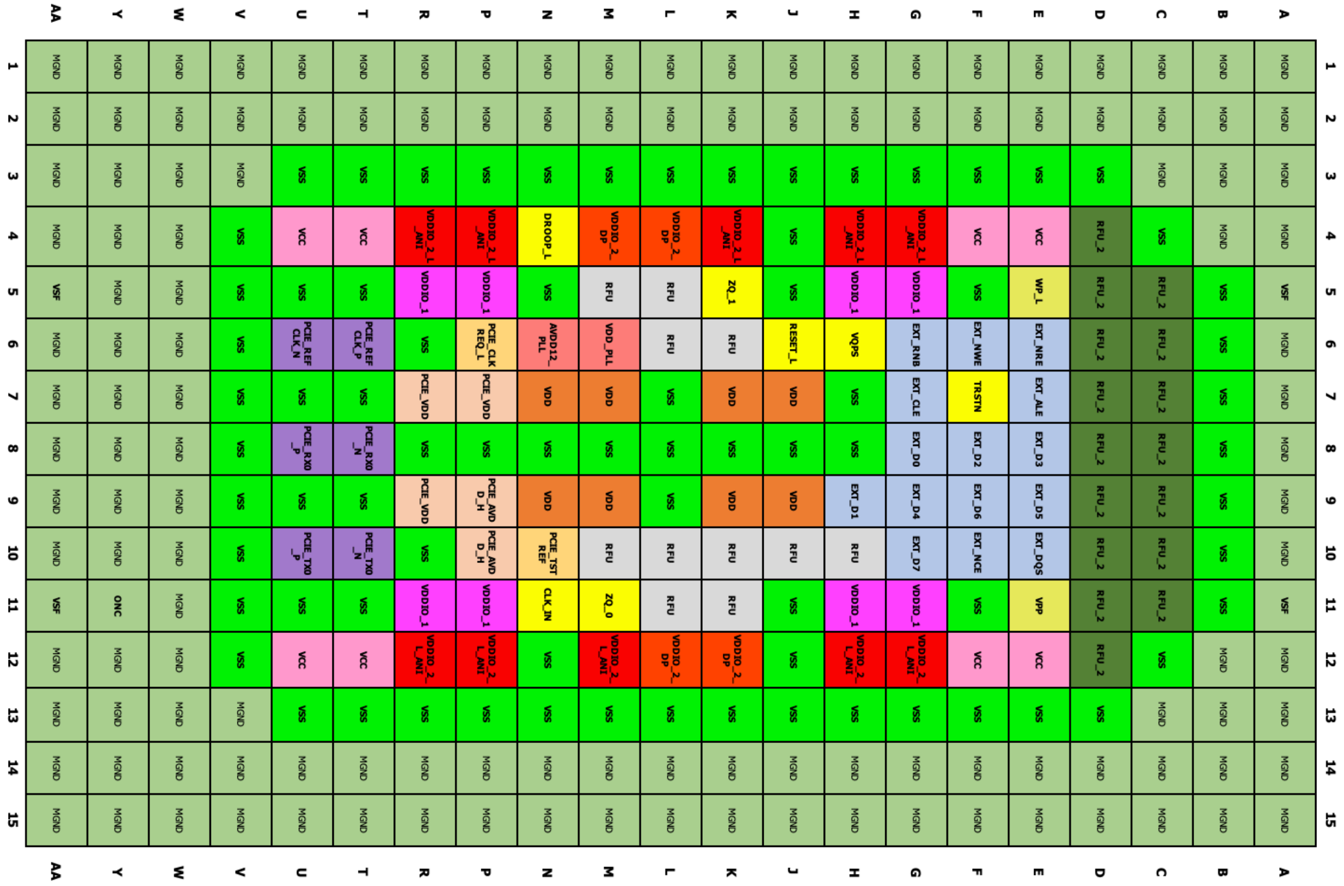
1.3.2. Marking Information

No		Code	
1	H	SK hynix	SK hynix
2	N	Product Family	Flash
3	3	Product Mode	Customized
4,5	G9 T0 T1 GQ GS T2 GV GT T3 T4	Product Density	G9 : 64GB T0 : 128GB GP : 192GB T1 : 256GB GQ : 320GB GS : 384GB T2 : 512GB GV : 576GB GT : 640GB T3 : 1TB T4 : 2TB
6	8 9 A B C D E F H	NAND Info	8 : 3DV4 256G 9 : 3DV4 512G A : 3DV5 512G B : 3DV6 512G C : 3DV6 1T D : 3DV7 512G F : 3DV8 512G H : 3DV9 1T
7	T	Cell Type	TLC
8	1 2 3 4 5 6 8 9 A G	Number of Die	1 : SDP 2 : DDP 3 : TDP 4 : QDP 5 : 5DP 6 : 6DP 8 : ODP 9 : 9DP A : 10DP G : 16DP
9	A B C D	Controller Name	A : S3E B : S4E C : S5E D : S6E
10	A	Client Name	Apple
11	X	Reserved	
12	Combination Code		
13			
14			

2. Physical Interface

2.1. Package Pin Layout

The S6E LGA has 315 pins, with the pin list and layout as shown below



	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	1
2	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	2
3	MGND	MGND	MGND	MGND	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MGND	MGND	MGND	3
4	MGND	MGND	MGND	VSS	VCC	VCC	VDDIO_2_L_ANI	VDDIO_2_L_ANI	DROOP_L	VDDIO_2_DP	VDDIO_2_DP	VDDIO_2_L_ANI	VSS	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VCC	VCC	RFU_2	VSS	MGND	MGND	4
5	VSF	MGND	MGND	VSS	VSS	VSS	VDDIO_1	VDDIO_1	VSS	RFU	RFU	ZQ_1	VSS	VDDIO_1	VDDIO_1	VSS	WP_L	RFU_2	RFU_2	VSS	VSF	5
6	MGND	MGND	MGND	VSS	PCIE_REF CLK_N	PCIE_REF CLK_P	VSS	PCIE_CLK REQ_L	AVDD12_PLL	VDD_PLL	RFU	RFU	RESET_L	VQPS	EXT_RNB	EXT_NWE	EXT_NRE	RFU_2	RFU_2	VSS	MGND	6
7	MGND	MGND	MGND	VSS	VSS	VSS	PCIE_VDD	PCIE_VDD	VDD	VDD	VSS	VDD	VDD	VSS	EXT_CLE	TRSTN	EXT_ALE	RFU_2	RFU_2	VSS	MGND	7
8	MGND	MGND	MGND	VSS	PCIE_RX0_P	PCIE_RX0_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	EXT_D0	EXT_D2	EXT_D3	RFU_2	RFU_2	VSS	MGND	8
9	MGND	MGND	MGND	VSS	VSS	VSS	PCIE_VDD	PCIE_AVDD_H	VDD	VDD	VSS	VDD	VDD	EXT_D1	EXT_D4	EXT_D6	EXT_D5	RFU_2	RFU_2	VSS	MGND	9
10	MGND	MGND	MGND	VSS	PCIE_TX0_P	PCIE_TX0_N	VSS	PCIE_AVDD_H	PCIE_TST REF	RFU	RFU	RFU	RFU	RFU	EXT_D7	EXT_NCE	EXT_DQS	RFU_2	RFU_2	VSS	MGND	10
11	VSF	ONC	MGND	VSS	VSS	VSS	VDDIO_1	VDDIO_1	CLK_IN	ZQ_0	RFU	RFU	VSS	VDDIO_1	VDDIO_1	VSS	VPP	RFU_2	RFU_2	VSS	VSF	11
12	MGND	MGND	MGND	VSS	VCC	VCC	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VSS	VDDIO_2_L_ANI	VDDIO_2_DP	VDDIO_2_DP	VSS	VDDIO_2_L_ANI	VDDIO_2_L_ANI	VCC	VCC	RFU_2	VSS	MGND	MGND	12
13	MGND	MGND	MGND	MGND	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MGND	MGND	MGND	13
14	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	14
15	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	15
	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 1: S6E Package LGA315 Pin Assignment

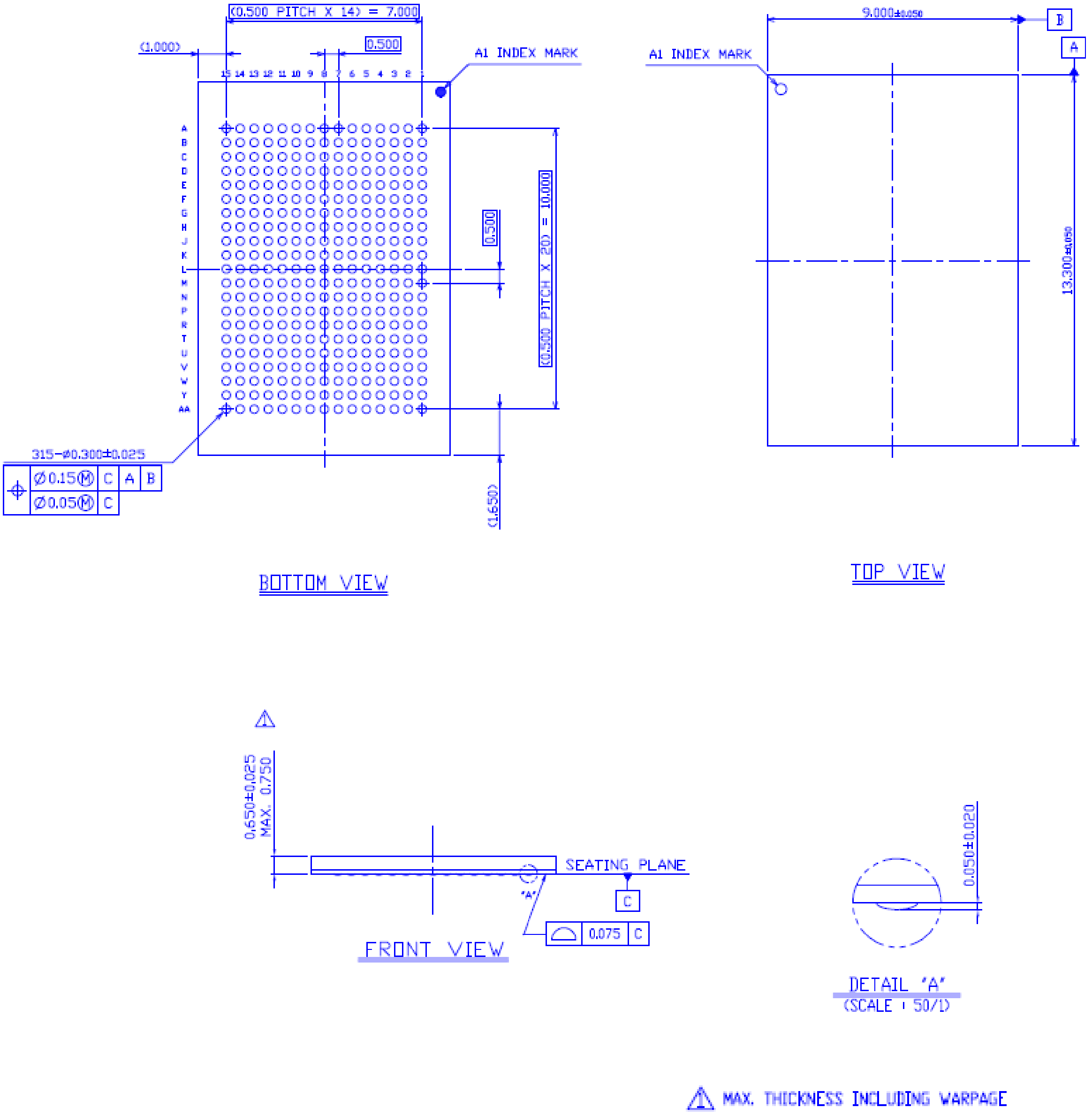
Package Pins	Usage in package	Comment
VDDIO_2_L_ANI	Same as VDDIO_2	NAND IF IO supply
VDDIO_2_DP	Same as VDDIO_2 Merged with VDDIO_2_L_ANI	Included in VDDIO_2_L_ANI for SIPI purpose *May separate beyond S6E package
RFU	Floating individually	Reserved for Future Use
RFU_2	Floating individually	Reserved for Future Use
Dummy	Tied to VSS	
Dummy*	Floating	*Y11 pin
VSF	- If vendor doesn't use VSF, these pins shall be shorted to VSS in package substrate - If vendor implement VSF connection to NAND die(s), 1. Vendor shall provide pre-notification and function of the pins to Apple, and need Apple approval before implementation 2. These pins in NAND die user mode shall be self-pulldown to VSS, or shall keep stable high-Z with characteristics confirmed with Apple 3. These pins in NAND die user mode shall be allowed to float or short to VSS, in Apple side usage 4. These pins also shall comply with ESD specifications	Vendor Specific Feature *A5, A11, AA5, AA11 pins

Table 2: Usage of VDDIO_2_L_ANI, VDDIO_2_DP, RFU, RFU_2, Dummy, Dummy* and VSF pins

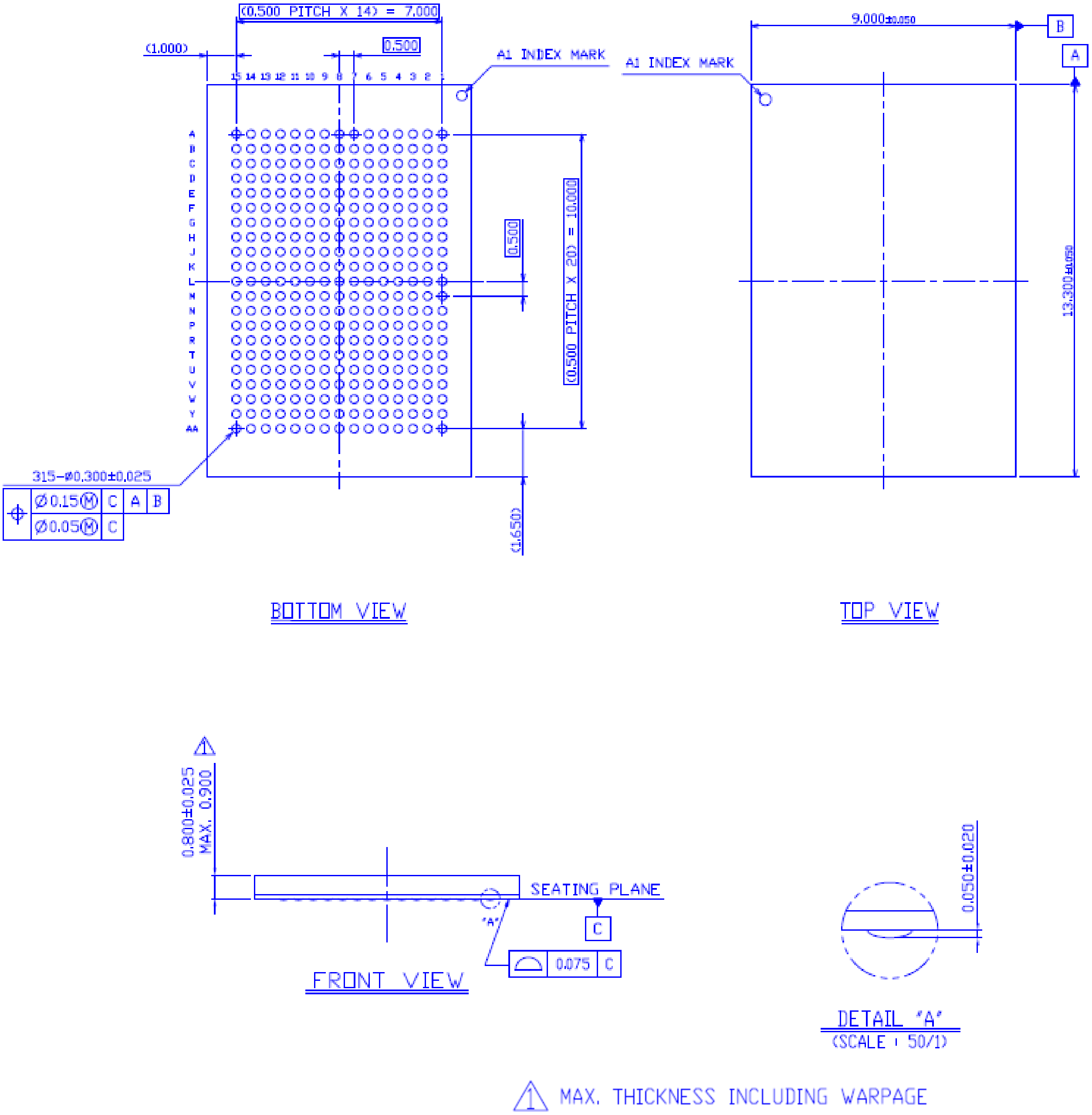
Number of NAND stack	X (mm)	Y (mm)	Z max (mm)	Body THK (mm)	Pre-bump (㎛)
1 / 2 / 4 / 8 die	13.3 (±0.05)	9.0 (±0.05)	0.75	0.65 (±0.025)	50 (±20)
16 die	13.3 (±0.05)	11.0 (±0.05)	0.9	0.8 (±0.025)	

APN	MPN	Number of NAND stack	Backend Location (City)	Backend Location (Nation)	Mass Production POR	Fab Information
335S00701	HN3T0HT1DAX430	1	CJ	Korea	No	M15 (CJ, Korea)
	HN3T0HT1DAX434	1	CQ	China	Yes	
335S00702	HN3T1HT2DAX437	2	CJ	Korea	Yes	
	HN3T1HT2DAX435	2	CQ	China	Yes	
335S00703	HN3T2HT4DAX431	4	CJ	Korea	Yes	
	HN3T2HT4DAX436	4	CQ	China	Yes	
335S00704	HN3T3HT8DAX431	8	CJ	Korea	Yes	
335S00714	HN3T4HTGDAX433	16	CJ	Korea	Yes	

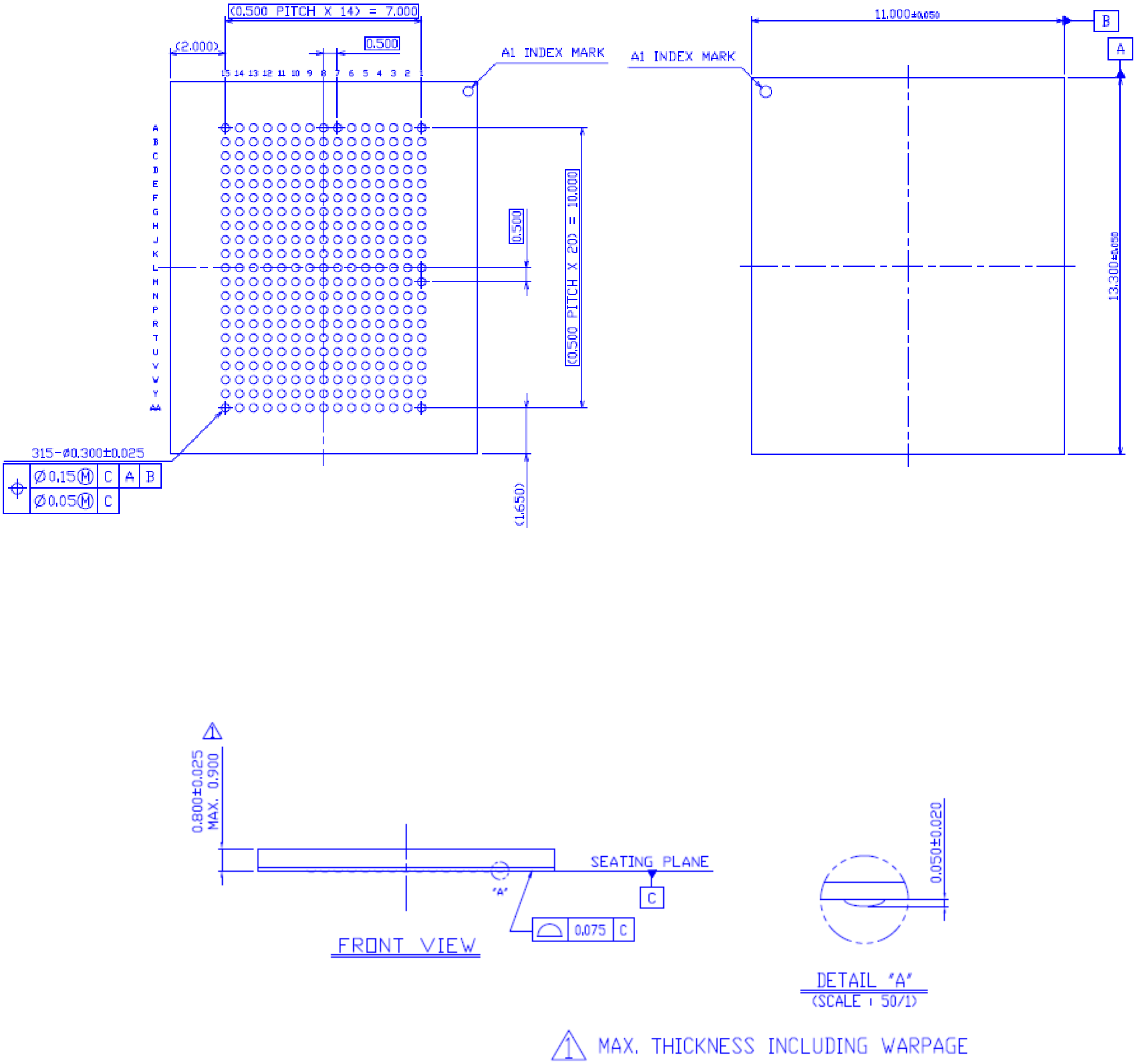
CJ - Cheongju, CQ: Chongqing



13.3x9.0x0.75mm LGA315 Package Outline Drawing



13.3x9.0x0.9mm LGA315 Package Outline Drawing



13.3x11.0x0.9mm LGA315 Package Outline Drawing