SAMSUNG

Rev. 1.0, Jul. 2024

KLBDG1N5DB-E0U30P9
KLBDG1N5DB-E0U3TP9
KLBEG2N5DB-E0U30P9
KLBEG2N5DB-E0U3TP9
KLBFG4N5DB-E0U30P9
KLBFG4N5DB-E0U3TP9
KLBGG8N5DB-E0U30P9
KLBGG8N5DB-E0U3TP9
KLBIGAN5DB-E0U30P9
KLBIGAN5DB-E0U3TP9
KLBFG4N5DB-E1U30P9
KLBFG4N5DB-E1U3TP9
KLBGG8N5DB-E1U30P9
KLBGG8N5DB-E1U3TP9

S5E NAND Flash B-die

Multi-Level-Cell (3bit/Cell)

Datasheet *For Apple*

Revision History

Revision No.	History	Draft Date	Remark	Edited by	Reviewed by
0.5	1. First version of specification for new revision mask of V8 1Tb.	5th Apr, 2024	Preliminary	H.K.Kim	J.M.Seok
0.6	1. 30um mold-gap height increased PKG 4/8DP(KLBFG4N5DB-E1U3xP9, KLBGG8N5DB-E1U3xP9) device information is added 2. In page 6, 16DP PKG size typo is corrected(13.3x9→13.3x11)	5th Jun, 2024	Preliminary	H.K.Kim	J.M.Seok
0.7	1. New Mask-New PKG 8DP PKG height is changed(0.93→0.9)	28th Jun, 2024	Preliminary	H.K.Kim	J.M.Seok
0.8	1. Distinguish Packing Type by Marked full Part Number(3xP9→30P9(Tray), 3TP9(T&R))	4th Jul, 2024	Preliminary	H.K.Kim	S.Y.Kang
0.9	1. Adding APN in datasheet	18th Jul, 2024	Preliminary	H.K.Kim	J.M.Seok
1.0	1. Adding Mask/PKG Condition for each MPN/APN	22nd Jul, 2024	Final	H.K.Kim	J.M.Seok

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Table Of Contents

1.0 INTRODUCTION

1.1 Product List for S5E

Part Number	APN	Mask/PKG Information	Density	Interface	V_{CC} Range	$V_{CC}Q$ Range	Organization	PCIe Gen.	PKG Type
KLBDG1N5DB-E0U30P9 KLBDG1N5DB-E0U3TP9	335S00710	New Mask + Old PKG	128GB	Toggle DDR	2.5V (2.35V ~ 2.75V)	1.2V (1.14V ~ 1.3V)	x8	4	315-LGA EMI Shielded
KLBEG2N5DB-E0U30P9 KLBEG2N5DB-E0U3TP9	335S00713	New Mask + Old PKG	256GB						
KLBFG4N5DB-E0U30P9 KLBFG4N5DB-E0U3TP9	335S00711	New Mask + Old PKG	512GB						
KLBGG8N5DB-E0U30P9 KLBGG8N5DB-E0U3TP9	335S00712	New Mask + Old PKG	1024GB						
KLBIGAN5DB-E0U30P9 KLBIGAN5DB-E0U3TP9	335S00709	New Mask + Old PKG	2048GB						
KLBFG4N5DB-E1U30P9 KLBFG4N5DB-E1U3TP9	335S00711	New Mask + New PKG	512GB						
KLBGG8N5DB-E1U30P9 KLBGG8N5DB-E1U3TP9	335S00712	New Mask + New PKG	1024GB						

1.2 Features

• Voltage Supply
- V_{CC}: 2.5V (2.35V ~ 2.75V)
- $V_{CC}Q$: 1.2 (1.14V ~ 1.3V)

• Organization of Single Die
- Page Size: (16K + 2K) x Byte
- Data Register: (16K + 2K) x Byte
- Block Size: 66.375M Byte
- Unit Device Capacity: 66.375M Byte x 2,224

• Products
- KLBDG1N5DB-E0U30P9/E0U3TP9 : 1 x Single NAND die
- KLBEG2N5DB-E0U30P9/E0U3TP9 : 2 x Single NAND die
- KLBFG4N5DB-E0U30P9/E0U3TP9 : 4 x Single NAND die
- KLBGG8N5DB-E0U30P9/E0U3TP9 : 8 x Single NAND die
- KLBIGAN5DB-E0U30P9/E0U3TP9 : 16 x Single NAND die
- KLBFG4N5DB-E1U30P9/E0U3TP9 : 4 x Single NAND die
- KLBGG8N5DB-E1U30P9/E0U3TP9 : 8 x Single NAND die

• Automatic Program and Erase
- Page Program: (16K + 2K) Byte
- Block Erase: 66.375M Byte

• Page Read Operation
- Random Read: 50μs (Typ.)
- Data Transfer Rate: up to 1.2Gbps ($V_{CC}Q$: 1.2V)

• Write Cycle Time
- Page Program Time: 330μs (Max)
- Block Erase Time: TBD (Typ.)

• Command / Address / Data Multiplexed DQ Port

• Toggle Mode DDR Data Interface

• Hardware Data Protection
- Program / Erase Lockout During Power Transitions

• Reliable CMOS Floating-Gate Technology
- ECC Requirement: LDPC Engine

• Command Driven Operation

• Scalable DQ Driver

• Randomizer function is required by controller

• Package
- KLBDG1N5DB-E0U30P9 : 315-LGA (Tray)
- KLBDG1N5DB-E0U3TP9 : 315-LGA (T&R)
- KLBEG2N5DB-E0U30P9 : 315-LGA (Tray)
- KLBEG2N5DB-E0U3TP9 : 315-LGA (T&R)
- KLBFG4N5DB-E0U30P9 : 315-LGA (Tray)
- KLBFG4N5DB-E0U3TP9 : 315-LGA (T&R)
- KLBGG8N5DB-E0U30P9 : 315-LGA (Tray)
- KLBGG8N5DB-E0U3TP9 : 315-LGA (T&R)
- KLBIGAN5DB-E0U30P9 : 315-LGA (Tray)
- KLBIGAN5DB-E0U3TP9 : 315-LGA (T&R)
- KLBFG4N5DB-E1U30P9 : 315-LGA (Tray)
- KLBFG4N5DB-E1U3TP9 : 315-LGA (T&R)
- KLBGG8N5DB-E1U30P9 : 315-LGA (Tray)
- KLBGG8N5DB-E1U3TP9 : 315-LGA (T&R)

2.0 PHYSICAL INTERFACES

In this section, all physical interface will be described (top-level block diagram, assignment and description of each pin, connectivity of the external pins).

2.1 Block Diagram

This section presents reference block diagram that describes S5E 1/2/4/8/16DP to NAND physical interface.

Connectivity schema#	Die Stack	S5E Mk2 PKG size (mm)	Total CH count	Total Bank count	#Bank/CH
1	16DP	13.3x11	2	4	2
2	8DP	13.3x9	2	2	1
3	8DP	13.3x9	2	4	2
4	1DP	Any	1	1	1

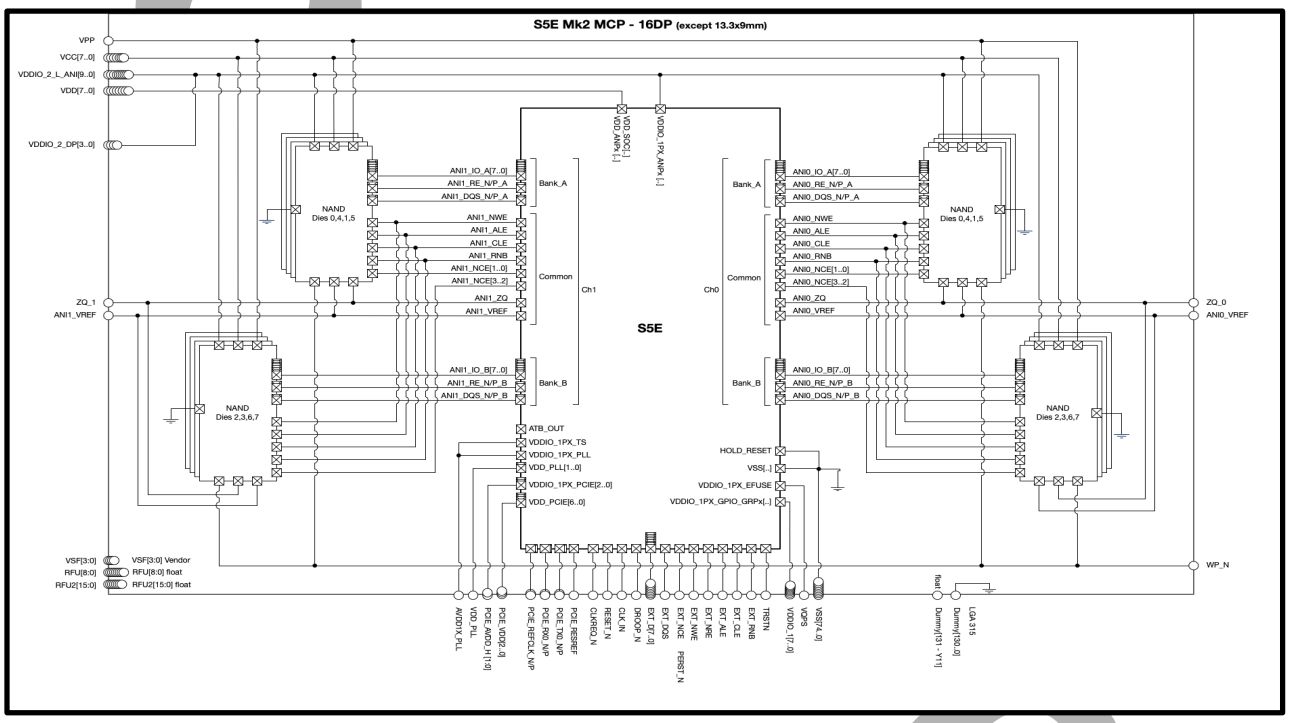


Figure 1. Connectivity schema #1

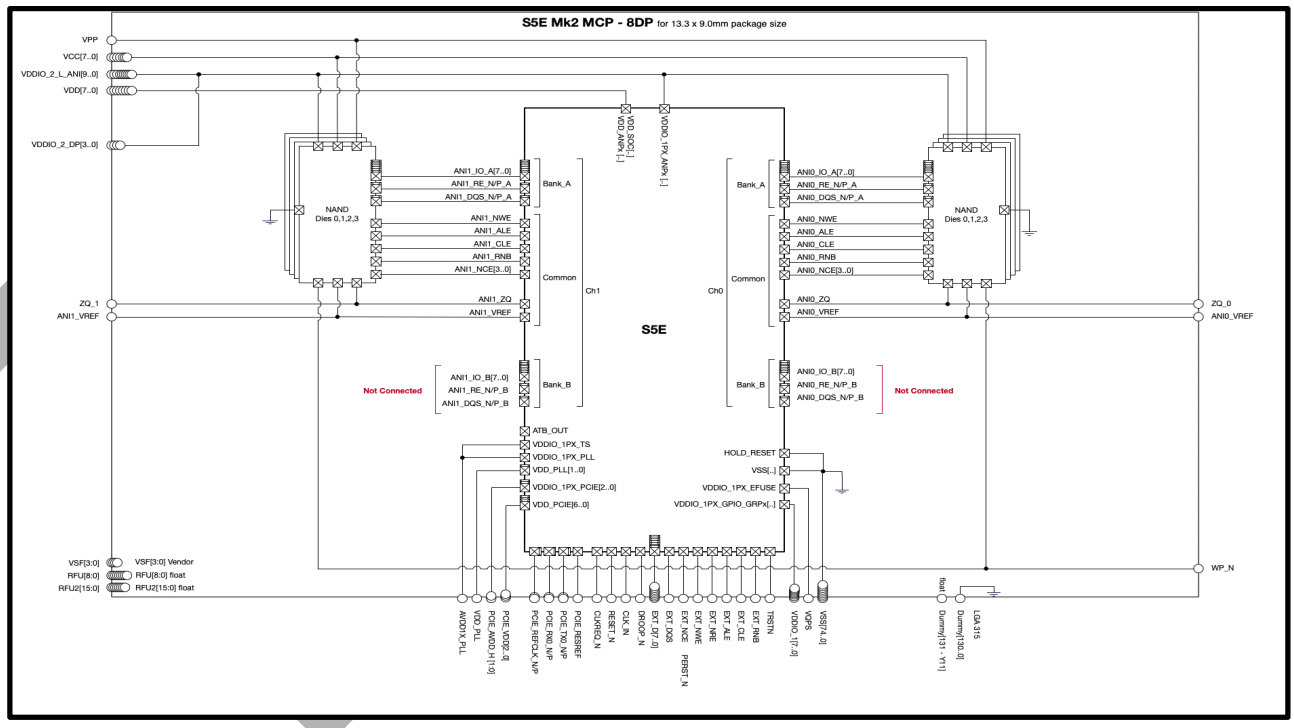


Figure 2. Connectivity schema #2

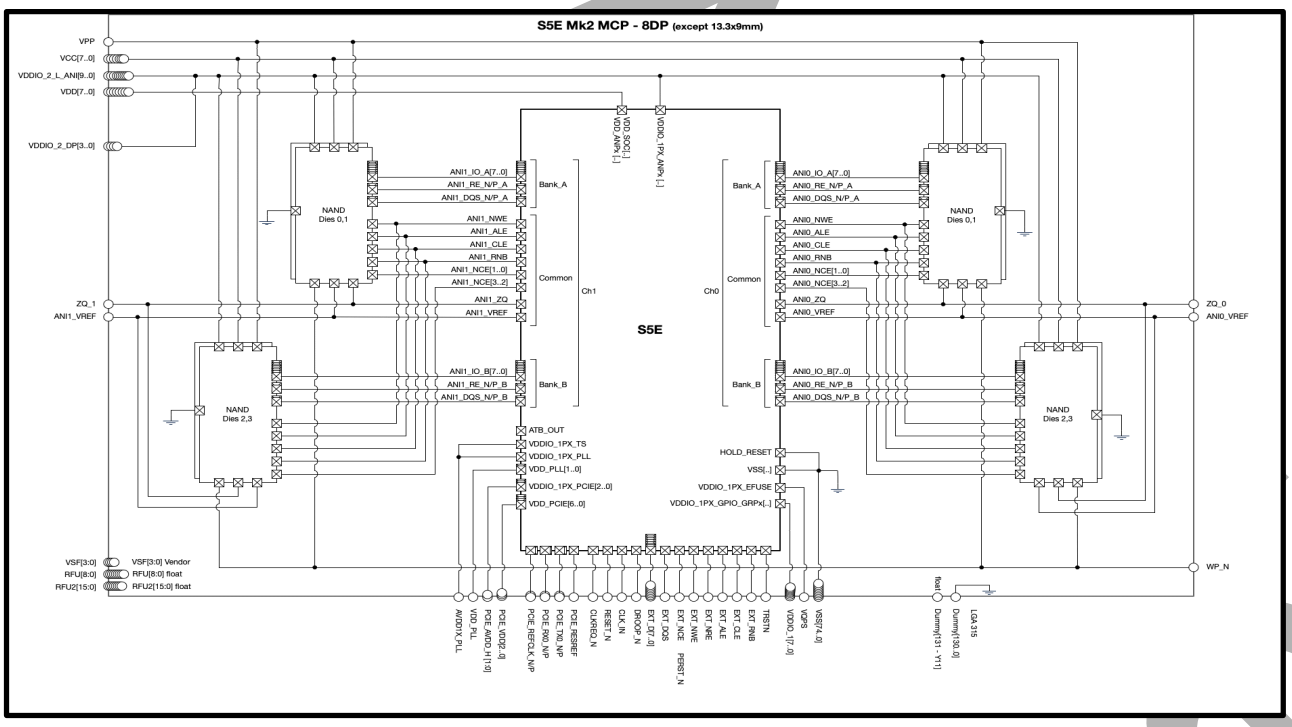


Figure 3. Connectivity schema #3

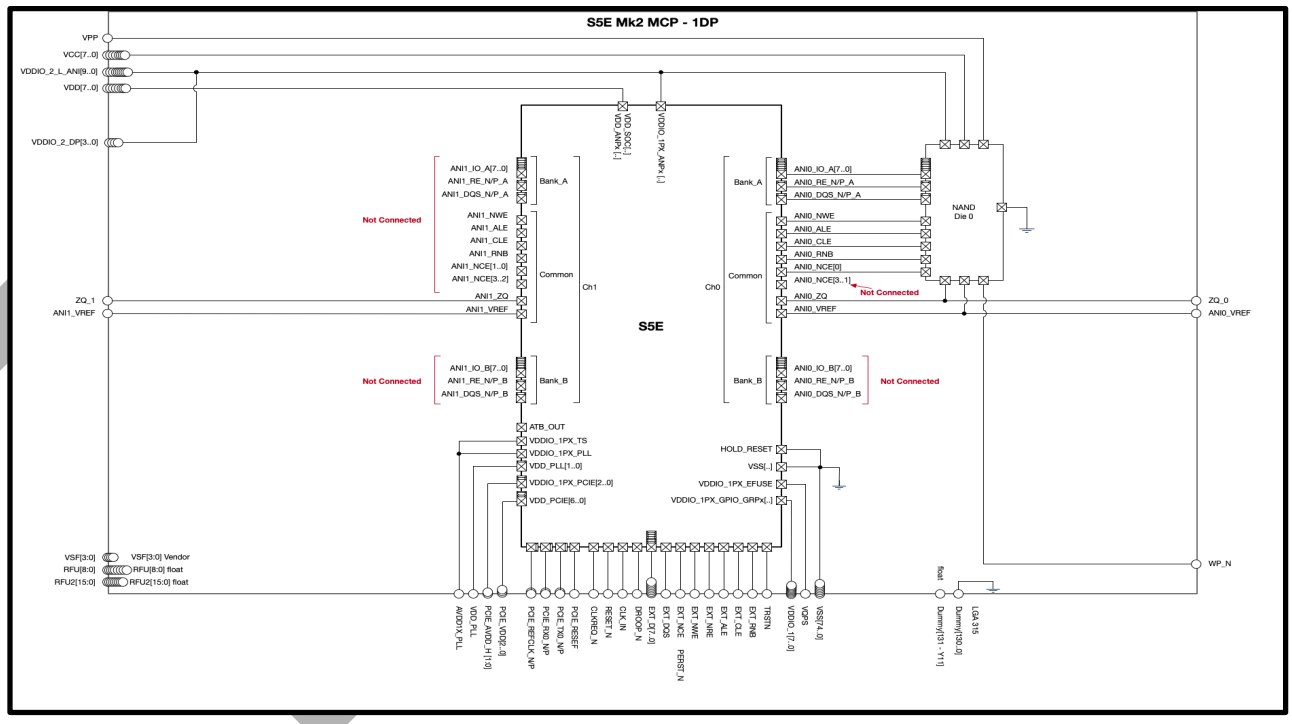


Figure 4. Connectivity schema #4

2.2 Pin Configuration (315-LGA)

This section includes a top view figure on MCP level. Each pin is placed in its physical location and with its logical assignment.
Figure 6 below is from S5E Mk2 NAND MCP Package Requirements. Table 1 below shows how to deal with Dummy, Dummy* and VSF pins in package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	Dummy	Dummy	Dummy	Dummy	VSF	Dummy	Dummy	Dummy	Dummy	Dummy	VSF	Dummy	Dummy	Dummy	Dummy	A
B	Dummy	Dummy	Dummy	Dummy	VSS	VSS	VSS	VSS	VSS	VSS	VSS	Dummy	Dummy	Dummy	Dummy	B
C	Dummy	Dummy	Dummy	VSS	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	VSS	Dummy	Dummy	Dummy	C
D	Dummy	Dummy	VSS	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU _pdate2	RFU_2	RFU_2	RFU_2	VSS	Dummy	Dummy	D
E	Dummy	Dummy	VSS	VCC	WP_N	EXT _NRE	EXT _ALE	EXT_D3	EXT_D5	EXT _DQS	VPP	VCC	VSS	Dummy	Dummy	E
F	Dummy	Dummy	VSS	VCC	VSS	EXT _NWE	TRSTN	EXT_D2	EXT_D6	EXT _NCE	VSS	VCC	VSS	Dummy	Dummy	F
G	Dummy	Dummy	VSS	VDDIO _2_L_ANI	VDDIO _1	EXT _RNB	EXT _CLE	EXT_D0	EXT_D4	EXT_D7	VDDIO _1	VDDIO_ 2_L_ANI	VSS	Dummy	Dummy	G
H	Dummy	Dummy	VSS	VDDIO _2_L_ANI	VDDIO _1	VQPS	VSS	VSS	EXT_D1	RFU	VDDIO _1	VDDIO_ 2_L_ANI	VSS	Dummy	Dummy	H
J	Dummy	Dummy	VSS	VSS	VSS	RESETN	VDD	VSS	VDD	RFU	VSS	VSS	VSS	Dummy	Dummy	J
K	Dummy	Dummy	VSS	VDDIO _2_L_ANI	ZQ_1	RFU	VDD	VSS	VDD	RFU	ANI0 _VREF	VDDIO _2_DP	VSS	Dummy	Dummy	K
L	Dummy	Dummy	VSS	VDDIO _2_DP	RFU	RFU	VSS	VSS	VSS	RFU	RFU	VDDIO _2_DP	VSS	Dummy	Dummy	L
M	Dummy	Dummy	VSS	VDDIO _2_DP	ANI1_V REF	VDD _PLL	VDD	VSS	VDD	RFU	ZQ_0	VDDIO _2_L_ANI	VSS	Dummy	Dummy	M
N	Dummy	Dummy	VSS	DROOP _N	VSS	AVDD1X _PLL	VDD	VSS	VDD	PCIE_R ESREF	CLK_IN	VSS	VSS	Dummy	Dummy	N
P	Dummy	Dummy	VSS	VDDIO _2_L_ANI	VDDIO _1	PCIE_C LKREQ_N	PCIE _VDD	VSS	PCIE _AVDD_H	PCIE _AVDD_H	VDDIO _1	VDDIO _2_L_ANI	VSS	Dummy	Dummy	P
R	Dummy	Dummy	VSS	VDDIO _2_L_ANI	VDDIO _1	VSS	PCIE _VDD	VSS	PCIE _VDD	VSS	VDDIO _1	VDDIO _2_L_ANI	VSS	Dummy	Dummy	R
T	Dummy	Dummy	VSS	VCC	VSS	PCIE _REFCLK _P	VSS	PCIE _RX0_N	VSS	PCIE _TX0_N	VSS	VCC	VSS	Dummy	Dummy	T
U	Dummy	Dummy	VSS	VCC	VSS	PCIE _REFCLK _N	VSS	PCIE _RX0_P	VSS	PCIE _TX0_P	VSS	VCC	VSS	Dummy	Dummy	U
V	Dummy	Dummy	Dummy	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	Dummy	Dummy	Dummy	V
W	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	W
Y	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy*	Dummy	Dummy	Dummy	Dummy	Y
AA	Dummy	Dummy	Dummy	Dummy	VSF	Dummy	Dummy	Dummy	Dummy	Dummy	VSF	Dummy	Dummy	Dummy	Dummy	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 5. S5E LGA315 Pin-out Assignments

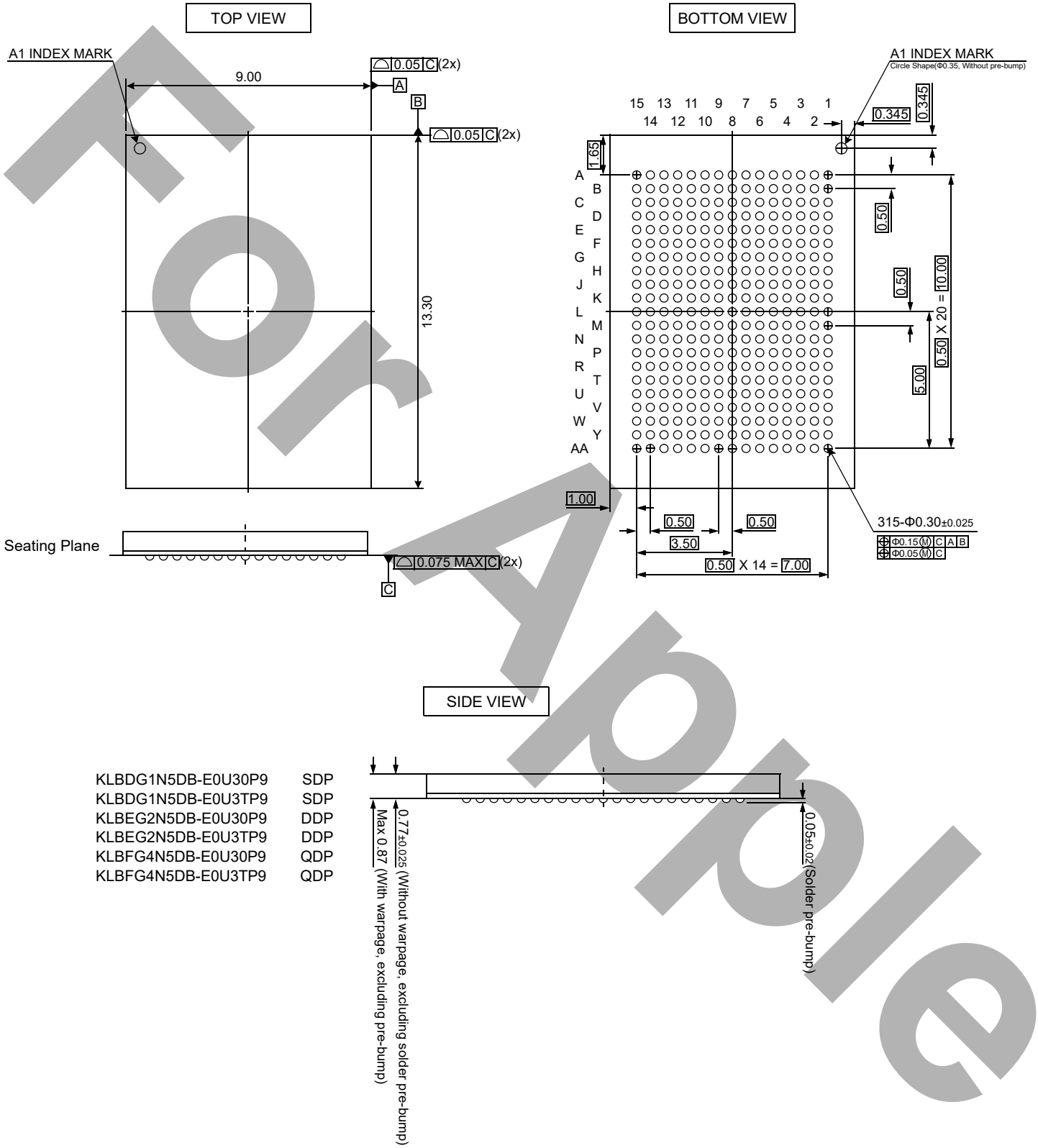
[Table 1] Usage of Dummy, Dummy* and VSF pins

Package Pins	Usage in package
Dummy	Tied to V_{SS}
Dummy*	Floating
VSF	Shorted to V_{SS} in package substrate

2.2.1 Package Dimensions

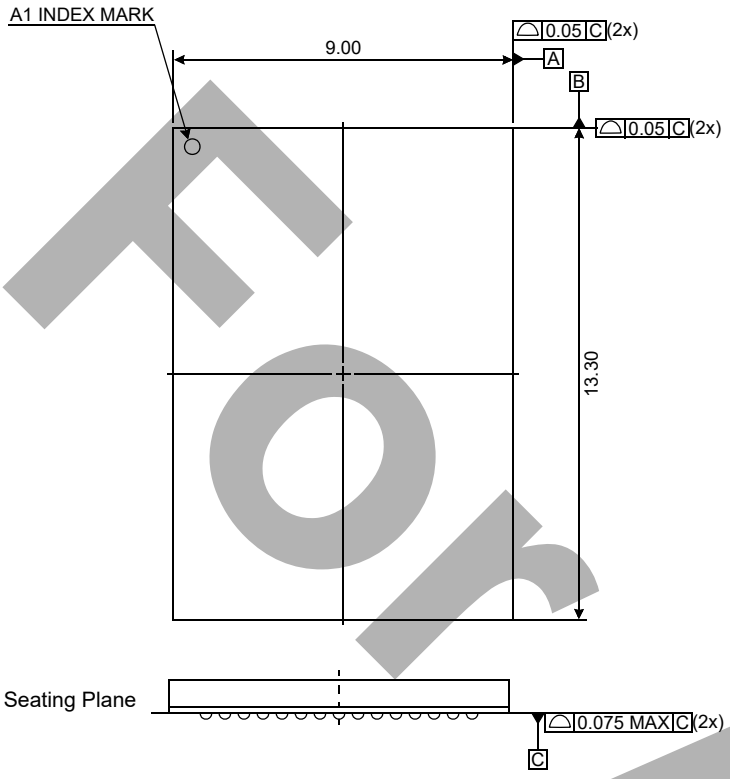
2.2.1.1 S5E Package Size

This package dimension drawing refers '210825_POD_S5E_9.0x13.3x0.87.pdf'

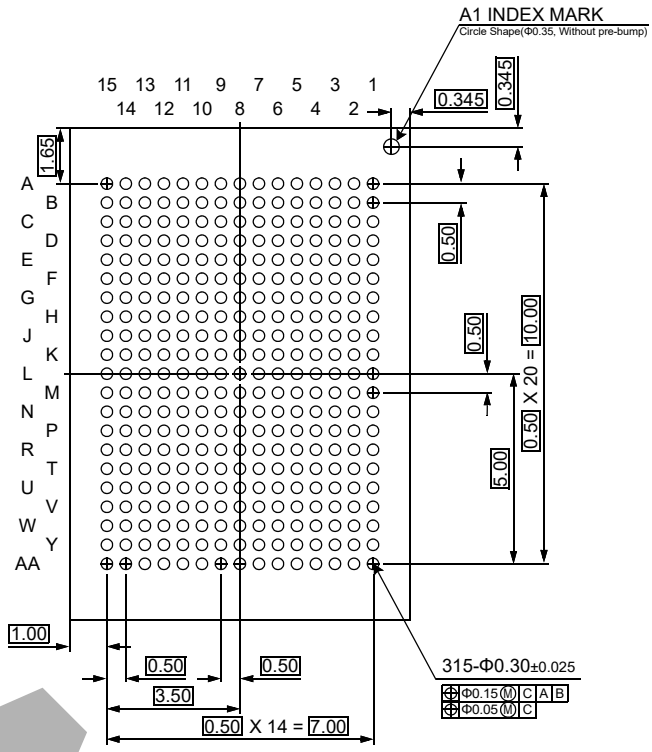


KLBDG1N5DB-E0U30P9	SDP
KLBDG1N5DB-E0U3TP9	SDP
KLBEG2N5DB-E0U30P9	DDP
KLBEG2N5DB-E0U3TP9	DDP
KLBFG4N5DB-E0U30P9	QDP
KLBFG4N5DB-E0U3TP9	QDP

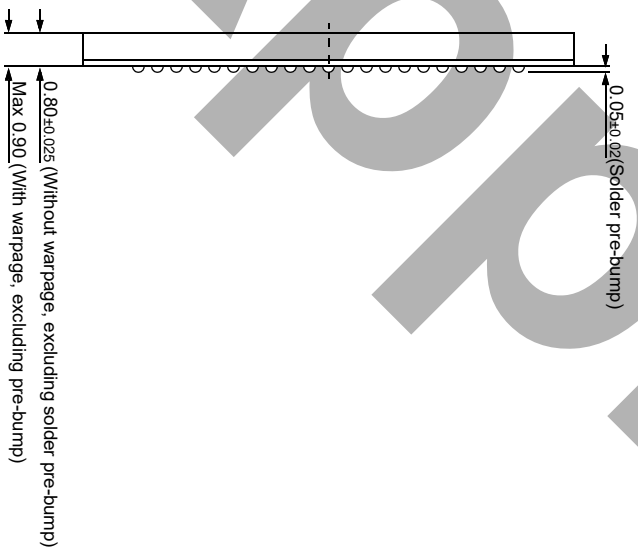
TOP VIEW



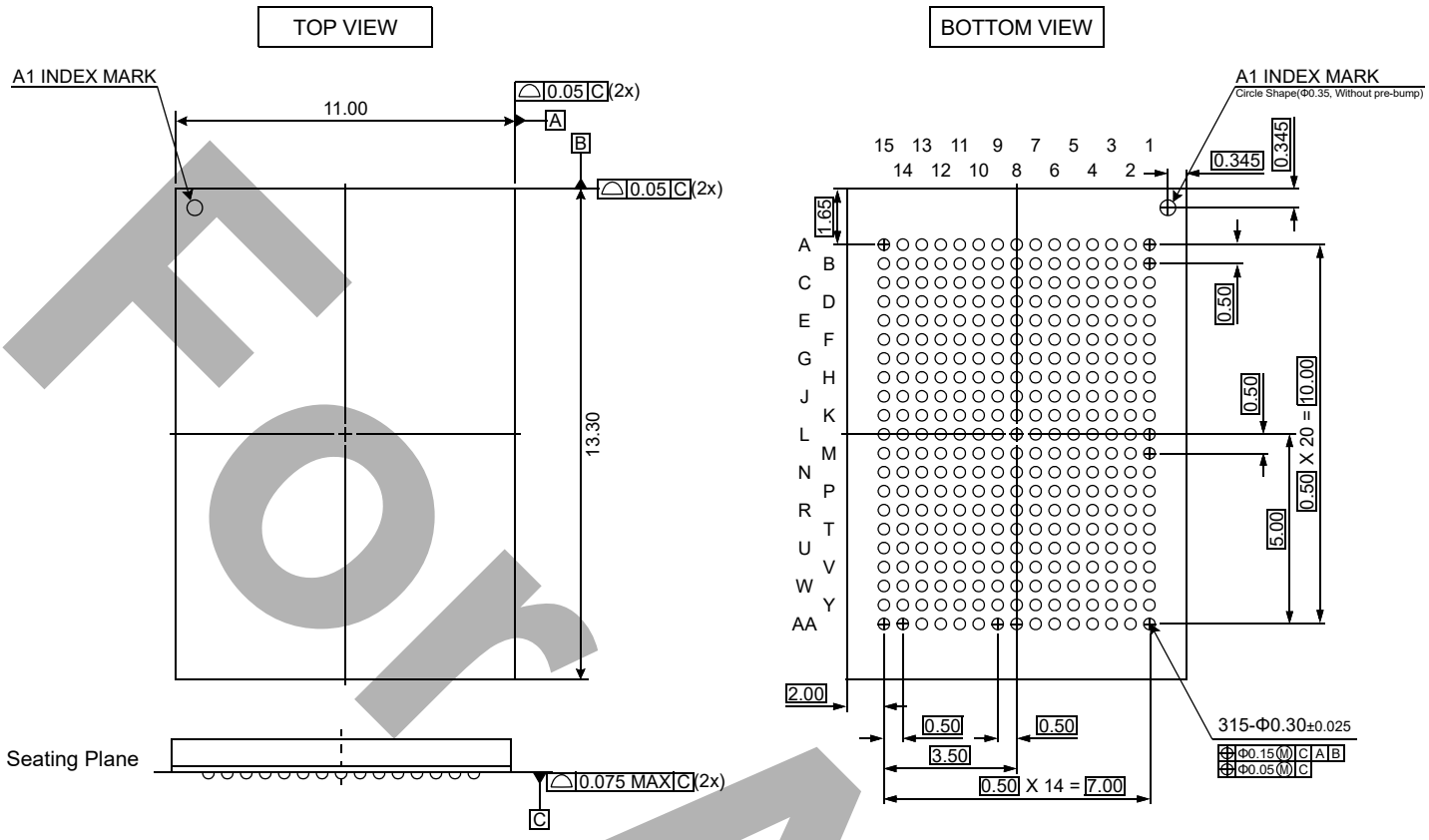
BOTTOM VIEW

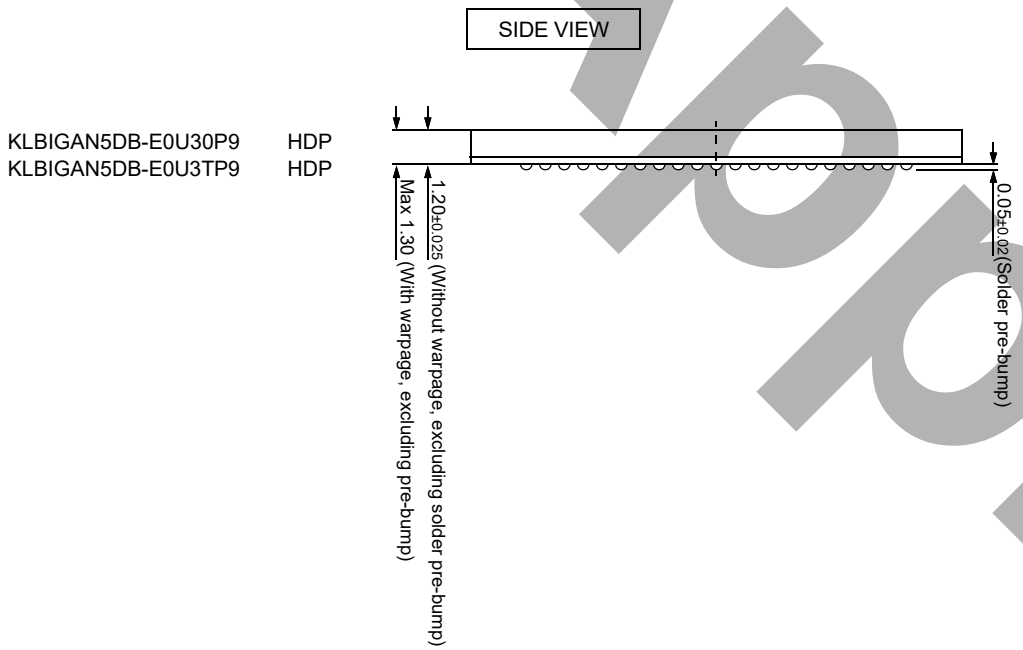


SIDE VIEW

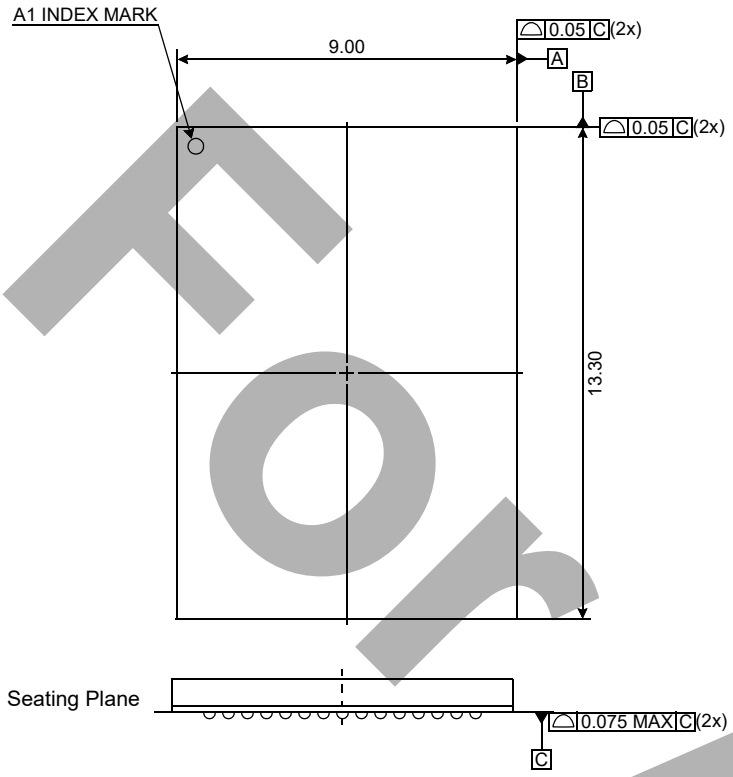


KLBGG8N5DB-E0U30P9	ODP
KLBGG8N5DB-E0U3TP9	ODP

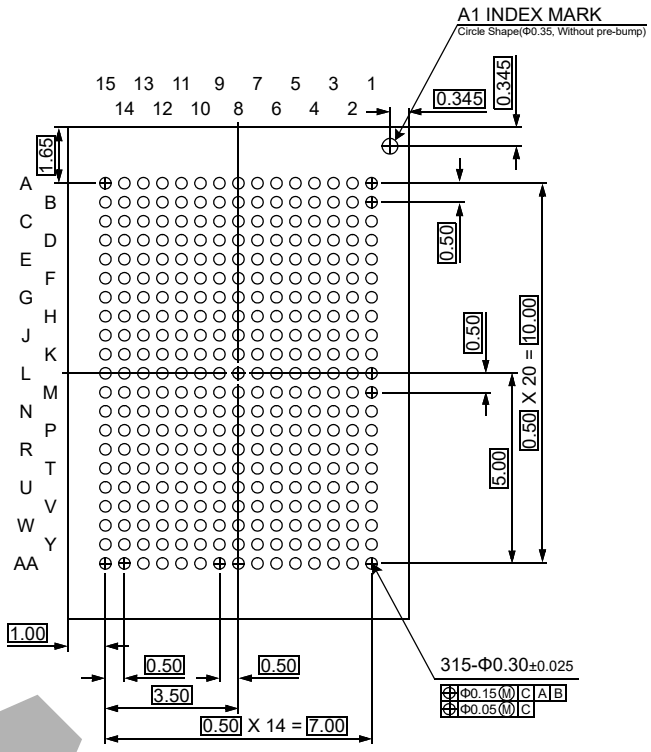

TOP VIEW
BOTTOM VIEW
A1 INDEX MARK
11.00
0.05 C (2x)
A
B
13.30
Seating Plane
0.075 MAX C (2x)
C
A1 INDEX MARK
Circle Shape(Φ0.35, Without pre-bump)
15 13 11 9 7 5 3 1
14 12 10 8 6 4 2
0.345
1.65
A B C D E F G H J K L M N P R T U V W Y AA
0.50
10.00 = 0.50 X 20
5.00
2.00
0.50
3.50
0.50 X 14 = 7.00
315-Φ0.30±0.025
Φ0.15 M C A B
Φ0.05 M C


SIDE VIEW
KLBIGAN5DB-E0U30P9 HDP
KLBIGAN5DB-E0U3TP9 HDP
Max 1.30 (With warpage, excluding pre-bump)
1.20±0.025 (Without warpage, excluding solder pre-bump)
0.05±0.02 (Solder pre-bump)

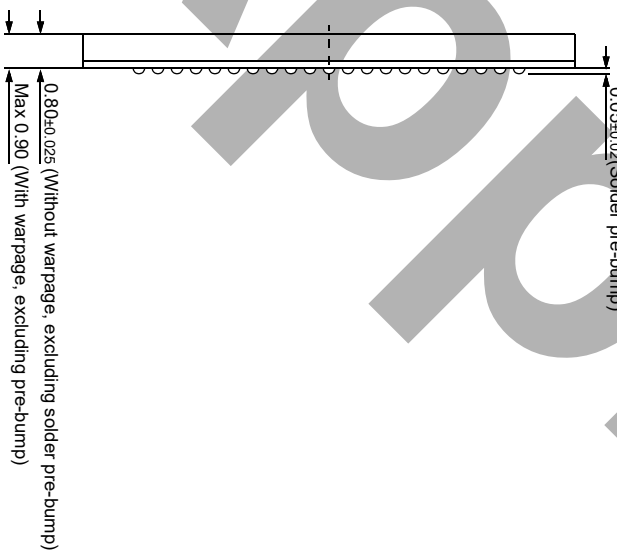
TOP VIEW



BOTTOM VIEW

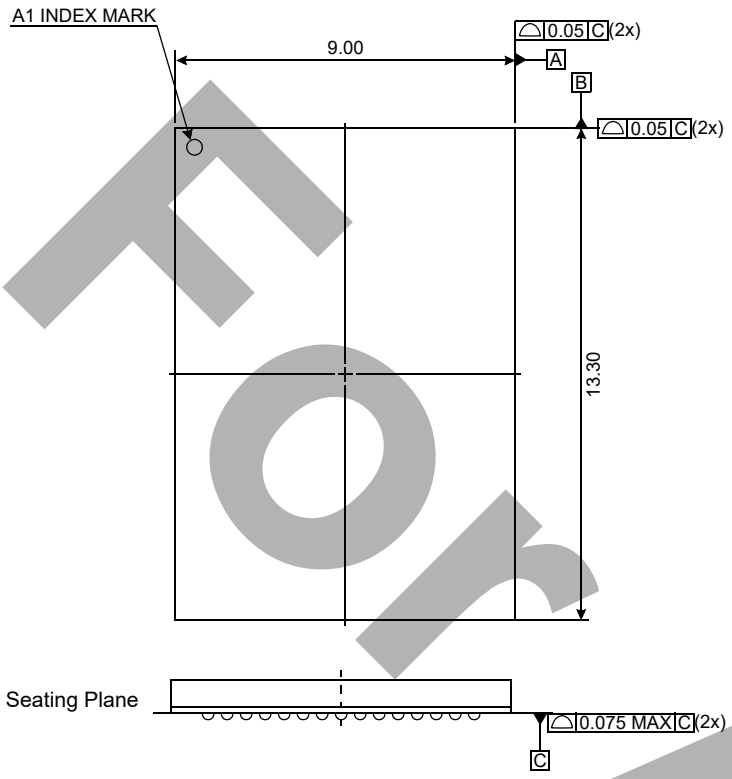


SIDE VIEW

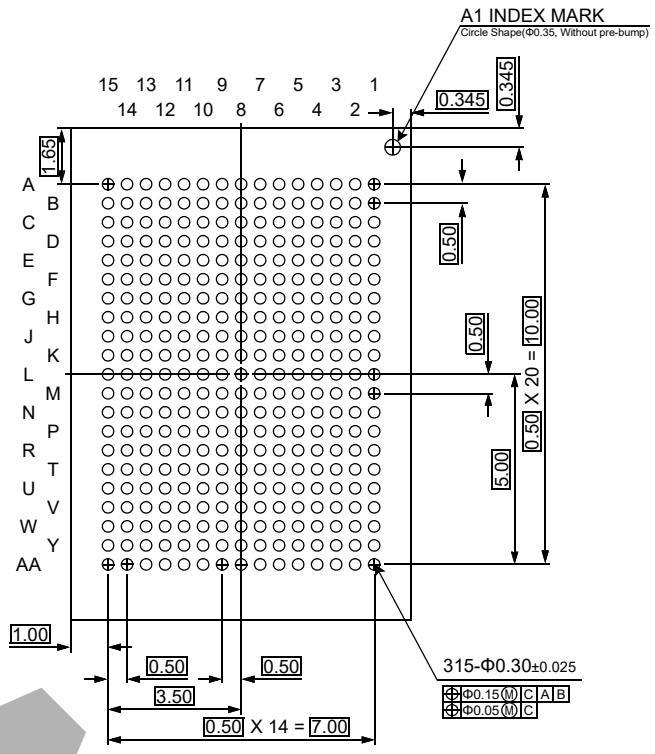


KLBFG4N5DB-E1U30P9	QDP
KLBFG4N5DB-E1U3TP9	QDP

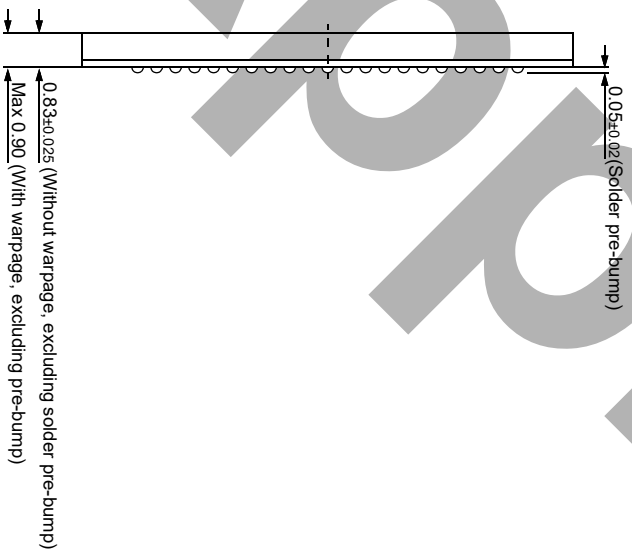
TOP VIEW



BOTTOM VIEW



SIDE VIEW



KLBGG8N5DB-E1U30P9	ODP
KLBGG8N5DB-E1U3TP9	ODP

The S5E package dimensions (X, Y, Body THK Norminal / Z Max including warpage and excluding pre-bump) for shielded.

Part Number	APN	Mask/PKG Information	Capacity	X (mm)	Y (mm)	Z (mm)	Body THK (mm)
KLBDG1N5DB-E0U30P9 KLBDG1N5DB-E0U3TP9	335S00710	New Mask + Old PKG	1 die	13.3	9	0.87[1)]	0.77
KLBEG2N5DB-E0U30P9 KLBEG2N5DB-E0U3TP9	335S00713	New Mask + Old PKG	2 die	13.3	9	0.87[1)]	0.77
KLBFG4N5DB-E0U30P9 KLBFG4N5DB-E0U3TP9	335S00711	New Mask + Old PKG	4 die	13.3	9	0.87[1)]	0.77
KLBGG8N5DB-E0U30P9 KLBGG8N5DB-E0U3TP9	335S00712	New Mask + Old PKG	8 die	13.3	9	0.9[2)]	0.8
KLBIGAN5DB-E0U30P9 KLBIGAN5DB-E0U3TP9	335S00709	New Mask + Old PKG	16 die	13.3	11.0	1.3[3)]	1.2
KLBFG4N5DB-E1U30P9 KLBFG4N5DB-E1U3TP9	335S00711	New Mask + New PKG	4 die	13.3	9	0.9[2)]	0.80
KLBGG8N5DB-E1U30P9 KLBGG8N5DB-E1U3TP9	335S00712	New Mask + New PKG	8 die	13.3	9	0.9[4)]	0.83

NOTE :
1) Max Z(THK) is 0.87mm (including warpage and excluding pre-bump).
2) Max Z(THK) is 0.9mm (including warpage and excluding pre-bump).
3) Max Z(THK) is 0.9mm (including warpage and excluding pre-bump).
4) Max Z(THK) is 1.3mm (including warpage and excluding pre-bump).

2.3 Pin Description

This section contains a table with names, direction and functionality description of all external pins.

[Table 2] S5E Signal Description (TBD)

Pin Name	Pin Function
VDDIO_2_DP	NAND IF IO supply
VDDIO_2_L_ANI	NAND IF IO supply
VDDIO_1	External interface supply
PCIE_AVDD_H	PCIE voltage supply
AVDD1X_PLL	PLL voltage supply
VQPS	Fuse burning supply (Only). Otherwise, connect to VSS
PCIE_VDD	PCIE digital supply
VDD_PLL	PLL digital supply
VDD	Core digital supply
VCC	Power supply to the NAND array (Not connected to controller)
VPP	NAND supply (Not connected to controller)
VSS	Global chip ground
PCIE_CLKREQ_N[1]	PCIe clock request. Active low.
PCIE_TX0_P	Differential TX lane 0
PCIE_TX0_N	
PCIE_RX0_P	Differential RX lane 0
PCIE_RX0_N	
PCIE_REFCLK_P	Differential PCIe PHY reference clock
PCIE_REFCLK_N	
PCI_RESREF	Reference pin. Requires 200Ω resistor. Should not be connected to lower resistance.
CLK_IN	24MHz reference clock
RESETN	Power-On-Reset and global reset, active low
ANI0_VREF [8]	ANI0 voltage reference source. May be an output (Internal VREF) or input (External VREF generated from on-board resistor ladder)
ANI1_VREF [8]	ANI1 voltage reference source. May be an output (Internal VREF) or input (External VREF generated from on-board resistor ladder)
ZQ_0 [8]	ANI0 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
ZQ_1 [8]	ANI1 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
WP_N	Write_Protect_N – Pin connected to NAND only
DROOP_N	DROOP_N – In functional mode, may be used as droop indication to SW.
EXT_D7 \ SPF_N	EXT_D7 in HW_BYPASS mode. The host channel 7th-bit, bidirectional port for transferring address, command, and data to and from the device SPF_N – Sudden Power Fail notification
EXT_D6 \ BOOT3	EXT_D6 in HW_BYPASS mode. The host channel 6th-bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap3 – Input enabled by default- for SW read.
EXT_D5 \ SPINAND_MOSI \ SPI_MOSI \ SWD_UID1	EXT_D5 in HW_BYPASS mode. The host channel 5th-bit, bidirectional port for transferring address, command, and data to and from the device. SPINAND_MOSI – SPI_MOSI pin in SPINAND mode SPI_MOSI – SPI_MOSI pin in SPI mode SWD_UID1 - Proprietary GPIO Unique ID1
EXT_D4 \ SPI_CS	EXT_D4 in HW_BYPASS mode. The host channel 4th-bit, bidirectional port for transferring address, command, and data to and from the device. SPI_CS – SPI Chip Select
EXT_D3 \ SPINAND_MISO \ SPI_MISO \ SWD_UID0	EXT_D3 in HW_BYPASS mode. The host channel 3rd-bit, bidirectional port for transferring address, command, and data to and from the device. SPINAND_MISO – SPI_MISO pin in SPINAND mode SPI_MISO – SPI_MISO pin in SPI mode SWD_UID0 - Proprietary GPIO Unique ID0
EXT_D2 \ BOOT2 \ SPINAND_SCLK \ SPI_SCLK	EXT_D2 in HW_BYPASS mode. The host channel 2nd-bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap2 – Input enabled by default- for SW read. SPINAND_SCLK – SPI_SCLK pin in SPINAND mode SPI_SCLK – SPI_SCLK pin in SPI mode

EXT_D1 \ BOOT1	EXT_D1 in HW_BYPASS mode. The host channel 1st-bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap1 – Input enabled by default- for SW read. GPIO – GPIO used as proprietary FW indication
EXT_D0 \ BOOT0	EXT_D0 in HW_BYPASS mode. The host channel 0th-bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap0 – Input enabled by default- for SW read.
EXT_DQS \ BCM_N	EXT_DQS in HW_BYPASS (DDR) mode. The data strobe signal that indicates the data valid window for the source synchronous data interface. Complementary signal is not in use. Pad disabled in bypass SDR mode BCM_N (Backward Compatibility Mode) bootstrap
EXT_NCE \ PERSTN	EXT_NCE in HW_BYPASS mode. The Chip Enable signal selects the target. When the Chip Enable is high and the target is in the Normal Ready mode, the target goes into an IDLE mode. When Chip Enable is low, the target is selected. PERSTN – In functional mode, PCIe side reset event. SW handled.
EXT_RNB \ JTAG_TDO	EXT_RnB in HW_BYPASS mode. Ready/Busy signal indicates the device status when the device executes legacy commands (read, erase, program and reset). When low, the signal indicates that one or more operations are in progress. JTAG_TDO – JTAG Test Data Out bit
EXT_NRE \ JTAG_TMS	EXT_NRE in HW_BYPASS mode. The Read Enable signal enables data output. JTAG_TMS – JTAG Test Mode Select bit
EXT_ALE \ JTAG_SEL	EXT_ALE in HW_BYPASS mode. The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). JTAG_SEL – JTAG Select bit
EXT_CLE \ JTAG_TDI	EXT_CLE in HW_BYPASS mode. The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). JTAG_TDI – JTAG Test Data In bit
EXT_NWE \ JTAG_TCK	EXT_NWE in HW_BYPASS mode. The Write Enable signal controls the latching of input data in the asynchronous data interface. Data, commands, and addresses are latched on the rising edge of WE#. JTAG_TCK – JTAG Clock bit
TRSTN	JTAG_TRSTN – JTAG Test Resetn.
RFU_2	Reserved for Future Use
Dummy	Dummy pin
VSF	Vendor Specific Function