

Target

S6E NAND Flash B-die

Multi-Level-Cell (3bit/Cell)

KLBDG1N5EB-F0V30P9
 KLBDG1N5EB-F0V3TP9
 KLBEG2N5EB-F0V30P9
 KLBEG2N5EB-F0V3TP9
 KLBFG4N5EB-F0V30P9
 KLBFG4N5EB-F0V3TP9
 KLBGG8N5EB-F0V30P9
 KLBGG8N5EB-F0V3TP9
 KLBIGAN5EB-F0V30P9
 KLBIGAN5EB-F0V3TP9
 KLBDG1N5EB-F1V30P9
 KLBDG1N5EB-F1V3TP9
 KLBEG2N5EB-F1V30P9
 KLBEG2N5EB-F1V3TP9
 KLBFG4N5EB-F1V30P9
 KLBFG4N5EB-F1V3TP9
 KLBGG8N5EB-F1V30P9
 KLBGG8N5EB-F1V3TP9
 KLBIGAN5EB-F1V30P9
 KLBIGAN5EB-F1V3TP9

Datasheet *For Apple*

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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Edited by</u>	<u>Reviewed by</u>
0.0	1. First version of specification for new revision mask of V8 1Tb.	9th Apr, 2024	Target	H.K.Kim	J.M.Seok
0.1	1. Distinguish Packing Type by Marked full Part Number(3xP9→30P9(Tray), 3TP9(T&R))	5th Jul, 2024	Target	H.K.Kim	J.M.Seok
0.2	1. Adding APN in datasheet	18th Jul, 2024	Target	H.K.Kim	J.M.Seok
0.3	1. Updated MPN for S6E A1 CTRL Revision.	19th Nov, 2024	Target	H.K.Kim	S.Y.Kang

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For Apple

1.0 INTRODUCTION

1.1 Product List for S6E

Part Number	S6E CTRL	APN	Density	Interface	V _{CC} Range	V _{CCQ} Range	Organization	PCIe Gen.	PKG Type
KLBDG1N5EB-F0V30P9 KLBDG1N5EB-F0V3TP9	A0	335S00699	128GB	Toggle DDR	2.5V (2.35V ~ 2.75V)	1.2V (1.14V ~ 1.3V)	x8	5	315-LGA EMI Shielded
KLBDG1N5EB-F1V30P9 KLBDG1N5EB-F1V3TP9	A1								
KLBEG2N5EB-F0V30P9 KLBEG2N5EB-F0V3TP9	A0	335S00683	256GB						
KLBEG2N5EB-F1V30P9 KLBEG2N5EB-F1V3TP9	A1								
KLBFG4N5EB-F0V30P9 KLBFG4N5EB-F0V3TP9	A0	335S00684	512GB						
KLBFG4N5EB-F1V30P9 KLBFG4N5EB-F1V3TP9	A1								
KLBGG8N5EB-F0V30P9 KLBGG8N5EB-F0V3TP9	A0	335S00685	1024GB						
KLBGG8N5EB-F1V30P9 KLBGG8N5EB-F1V3TP9	A1								
KLBIGAN5EB-F0V30P9 KLBIGAN5EB-F0V3TP9	A0	335S00686	2048GB						
KLBIGAN5EB-F1V30P9 KLBIGAN5EB-F1V3TP9	A1								

1.2 Features

- Voltage Supply
 - V_{CC} : 2.5V (2.35V ~ 2.75V)
 - V_{CCQ} : 1.2 (1.14V ~ 1.3V)
- Organization of Single Die
 - Page Size: (16K + 2K) x Byte
 - Data Register: (16K + 2K) x Byte
 - Block Size: 66.375M Byte
 - Unit Device Capacity: 66.375M Byte x 2,224
- Products
 - KLBBDG1N5EB-F0V30P9/F0V3TP9/F1V30P9/F1V3TP9: 1 x Single NAND die
 - KLBEG2N5EB-F0V30P9/F0V3TP9/F1V30P9/F1V3TP9: 2 x Single NAND die
 - KLBFG4N5EB-F0V30P9/F0V3TP9/F1V30P9/F1V3TP9: 4 x Single NAND die
 - KLBGG8N5EB-F0V30P9/F0V3TP9/F1V30P9/F1V3TP9: 8 x Single NAND die
 - KLBIGAN5EB-F0V30P9/F0V3TP9/F1V30P9/F1V3TP9: 16 x Single NAND die
- Automatic Program and Erase
 - Page Program: (16K + 2K) Byte
 - Block Erase: 66.375M Byte
- Page Read Operation
 - Random Read: TBD (Typ.)
 - Data Transfer Rate: up to 2.4Gbps (V_{CCQ} : 1.2V)
- Write Cycle Time
 - Page Program Time: TBD (5 σ)
 - Block Erase Time: TBD (Typ.)
- Command / Address / Data Multiplexed DQ Port
- Toggle Mode DDR Data Interface
- Hardware Data Protection
 - Program / Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
 - ECC Requirement: LDPC Engine
- Command Driven Operation
- Scalable DQ Driver
- Randomizer function is required by controller
- Package
 - KLBBDG1N5EB-F0V30P9: 315-LGA (Tray)
 - KLBBDG1N5EB-F0V3TP9: 315-LGA(T&R)
 - KLBBDG1N5EB-F1V30P9: 315-LGA (Tray)
 - KLBBDG1N5EB-F1V3TP9: 315-LGA(T&R)
 - KLBEG2N5EB-F0V30P9: 315-LGA (Tray)
 - KLBEG2N5EB-F0V3TP9: 315-LGA (T&R)
 - KLBEG2N5EB-F1V30P9: 315-LGA (Tray)
 - KLBEG2N5EB-F1V3TP9: 315-LGA (T&R)
 - KLBFG4N5EB-F0V30P9: 315-LGA (Tray)
 - KLBFG4N5EB-F0V3TP9: 315-LGA (T&R)
 - KLBFG4N5EB-F1V30P9: 315-LGA (Tray)
 - KLBFG4N5EB-F1V3TP9: 315-LGA (T&R)
 - KLBGG8N5EB-F0V30P9: 315-LGA (Tray)
 - KLBGG8N5EB-F0V3TP9: 315-LGA (T&R)
 - KLBGG8N5EB-F1V30P9: 315-LGA (Tray)
 - KLBGG8N5EB-F1V3TP9: 315-LGA (T&R)
 - KLBIGAN5EB-F0V30P9: 315-LGA (Tray)
 - KLBIGAN5EB-F0V3TP9: 315-LGA (T&R)
 - KLBIGAN5EB-F1V30P9: 315-LGA (Tray)
 - KLBIGAN5EB-F1V3TP9: 315-LGA (T&R)

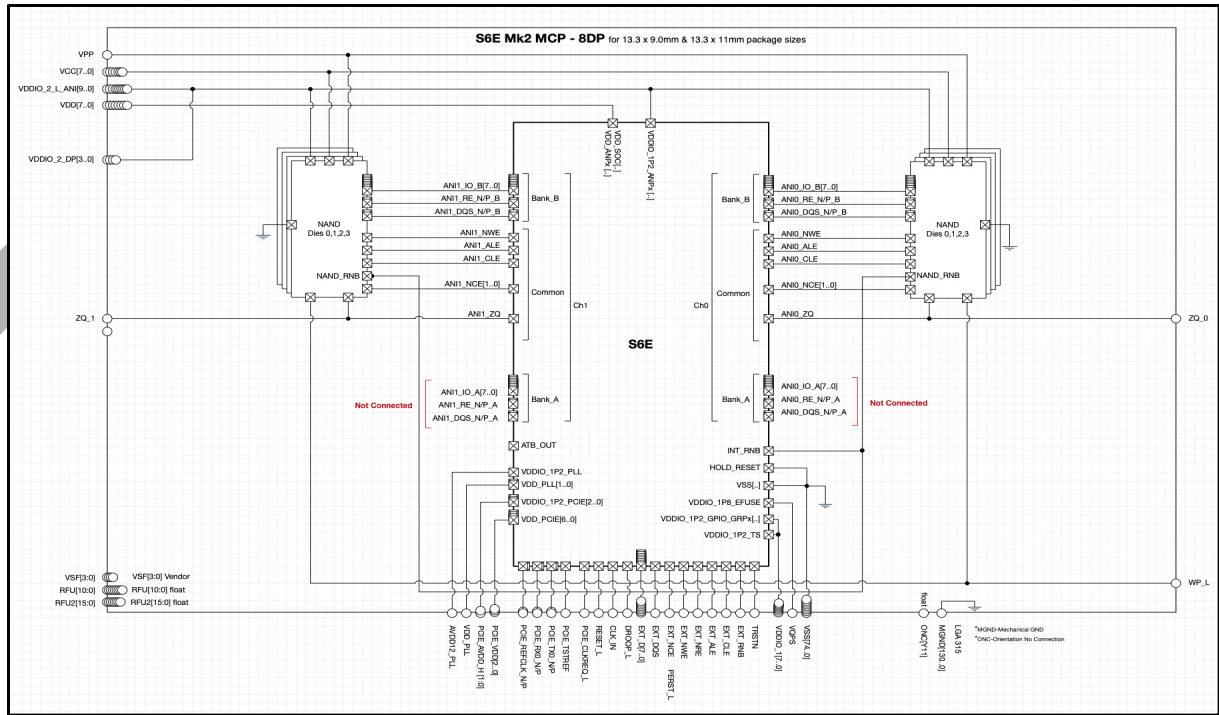


Figure 2. Connectivity schema #2

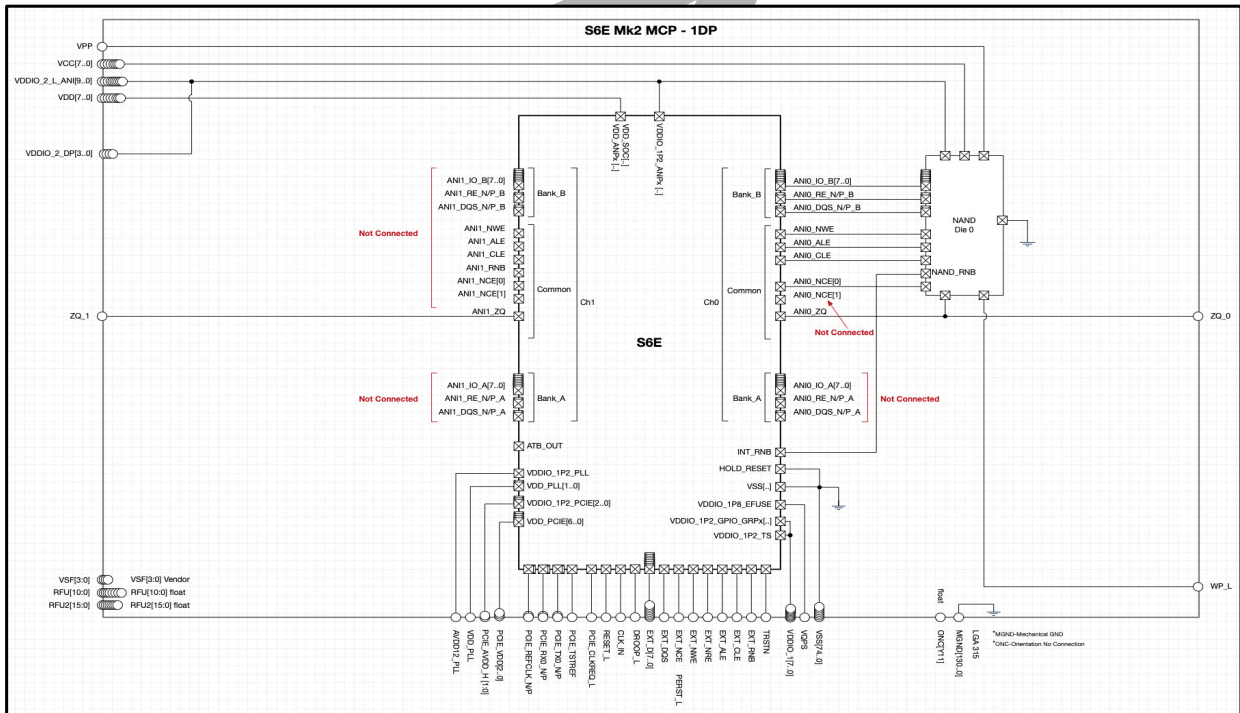


Figure 3. Connectivity schema #3

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2.2 Pin Configuration (315-LGA)

This section includes a top view figure on MCP level. Each pin is placed in its physical location and with its logical assignment.

Figure 6 below is from S6E Mk2 NAND MCP Package Requirements. Table 1 below shows how to deal with MGND, MGND* and VSF pins in package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	MGND	MGND	MGND	MGND	VSF	MGND	MGND	MGND	MGND	MGND	VSF	MGND	MGND	MGND	MGND	A
B	MGND	MGND	MGND	MGND	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MGND	MGND	MGND	MGND	B
C	MGND	MGND	MGND	VSS	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	VSS	MGND	MGND	MGND	C
D	MGND	MGND	VSS	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	RFU_2	VSS	MGND	MGND	D
E	MGND	MGND	VSS	VCC	WP_L	EXT_NRE	EXT_ALE	EXT_D3	EXT_D5	EXT_DQS	VPP	VCC	VSS	MGND	MGND	E
F	MGND	MGND	VSS	VCC	VSS	EXT_NWE	TRSTN	EXT_D2	EXT_D6	EXT_NCE	VSS	VCC	VSS	MGND	MGND	F
G	MGND	MGND	VSS	VDDIO_2_L_ANI	VDDIO_1	EXT_RNB	EXT_CLE	EXT_D0	EXT_D4	EXT_D7	VDDIO_1	VDDIO_2_L_ANI	VSS	MGND	MGND	G
H	MGND	MGND	VSS	VDDIO_2_L_ANI	VDDIO_1	VQPS	VSS	VSS	EXT_D1	RFU	VDDIO_1	VDDIO_2_L_ANI	VSS	MGND	MGND	H
J	MGND	MGND	VSS	VSS	VSS	RESET_L	VDD	VSS	VDD	RFU	VSS	VSS	VSS	MGND	MGND	J
K	MGND	MGND	VSS	VDDIO_2_L_ANI	ZQ_1	RFU	VDD	VSS	VDD	RFU	RFU	VDDIO_2_DP	VSS	MGND	MGND	K
L	MGND	MGND	VSS	VDDIO_2_DP	RFU	RFU	VSS	VSS	VSS	RFU	RFU	VDDIO_2_DP	VSS	MGND	MGND	L
M	MGND	MGND	VSS	VDDIO_2_DP	RFU	VDD_PLL	VDD	VSS	VDD	RFU	ZQ_0	VDDIO_2_L_ANI	VSS	MGND	MGND	M
N	MGND	MGND	VSS	DROOP_L	VSS	AVDD12_PLL	VDD	VSS	VDD	PCIE_TSTREF	CLK_IN	VSS	VSS	MGND	MGND	N
P	MGND	MGND	VSS	VDDIO_2_L_ANI	VDDIO_1	PCIE_CLKREQ_L	PCIE_VDD	VSS	PCIE_AVDD_H	PCIE_AVDD_H	VDDIO_1	VDDIO_2_L_ANI	VSS	MGND	MGND	P
R	MGND	MGND	VSS	VDDIO_2_L_ANI	VDDIO_1	VSS	PCIE_VDD	VSS	PCIE_VDD	VSS	VDDIO_1	VDDIO_2_L_ANI	VSS	MGND	MGND	R
T	MGND	MGND	VSS	VCC	VSS	PCIE_REFCLK_P	VSS	PCIE_RX0_N	VSS	PCIE_TX0_N	VSS	VCC	VSS	MGND	MGND	T
U	MGND	MGND	VSS	VCC	VSS	PCIE_REFCLK_N	VSS	PCIE_RX0_P	VSS	PCIE_TX0_P	VSS	VCC	VSS	MGND	MGND	U
V	MGND	MGND	MGND	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MGND	MGND	MGND	V
W	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	W
Y	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	MGND	ONC	MGND	MGND	MGND	MGND	Y
AA	MGND	MGND	MGND	MGND	VSF	MGND	MGND	MGND	MGND	MGND	VSF	MGND	MGND	MGND	MGND	AA

Figure 4. S6E LGA315 Pin-out Assignments

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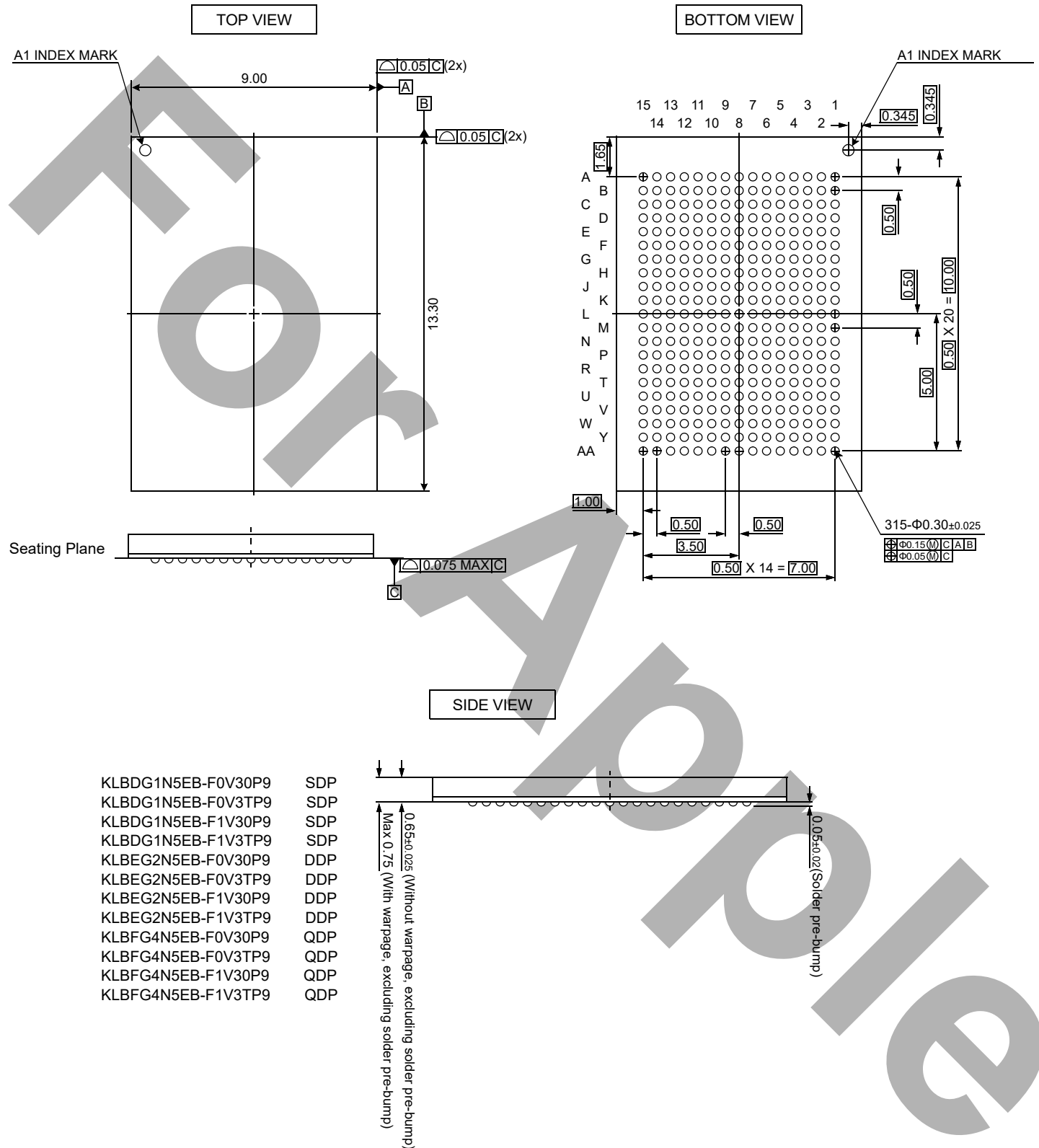
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[Table 1] Usage of VDDIO_2_L_ANI, VDDIO_2_DP, RFU, RFU_2, MGND, ONC, and VSF pins

Package Pins	Usage in package	Comment
VDDIO_2_L_ANI	Same as VDDIO_2	NAND IF IO supply
VDDIO_2_DP	Same as VDDIO_2 Merged with VDDIO_2_L_ANI	Included in VDDIO_2_L_ANI for SIPI purpose *May separate beyond S6E package
RFU	Floating individually	Reserved for Future Use
RFU_2	Floating individually	Reserved for Future Use
MGND	Tied to VSS	
ONC	Floating	*Y11 pin
VSF	- If vendor doesn't use VSF, these pins shall be shorted to VSS in package substrate - If vendor implement VSF connection to NAND die(s), 1. Vendor shall provide pre-notification and function of the pins to Apple, and need Apple approval before implementation 2. These pins in NAND die user mode shall be self-pulldown to VSS, or shall keep stable high-Z with characteristics confirmed with Apple 3. These pins in NAND die user mode shall be allowed to float or short to VSS, in Apple side usage 4. These pins also shall comply with ESD specifications	Vendor Specific Feature *A5, A11, AA5, AA11 pins

2.2.1 Package Dimensions

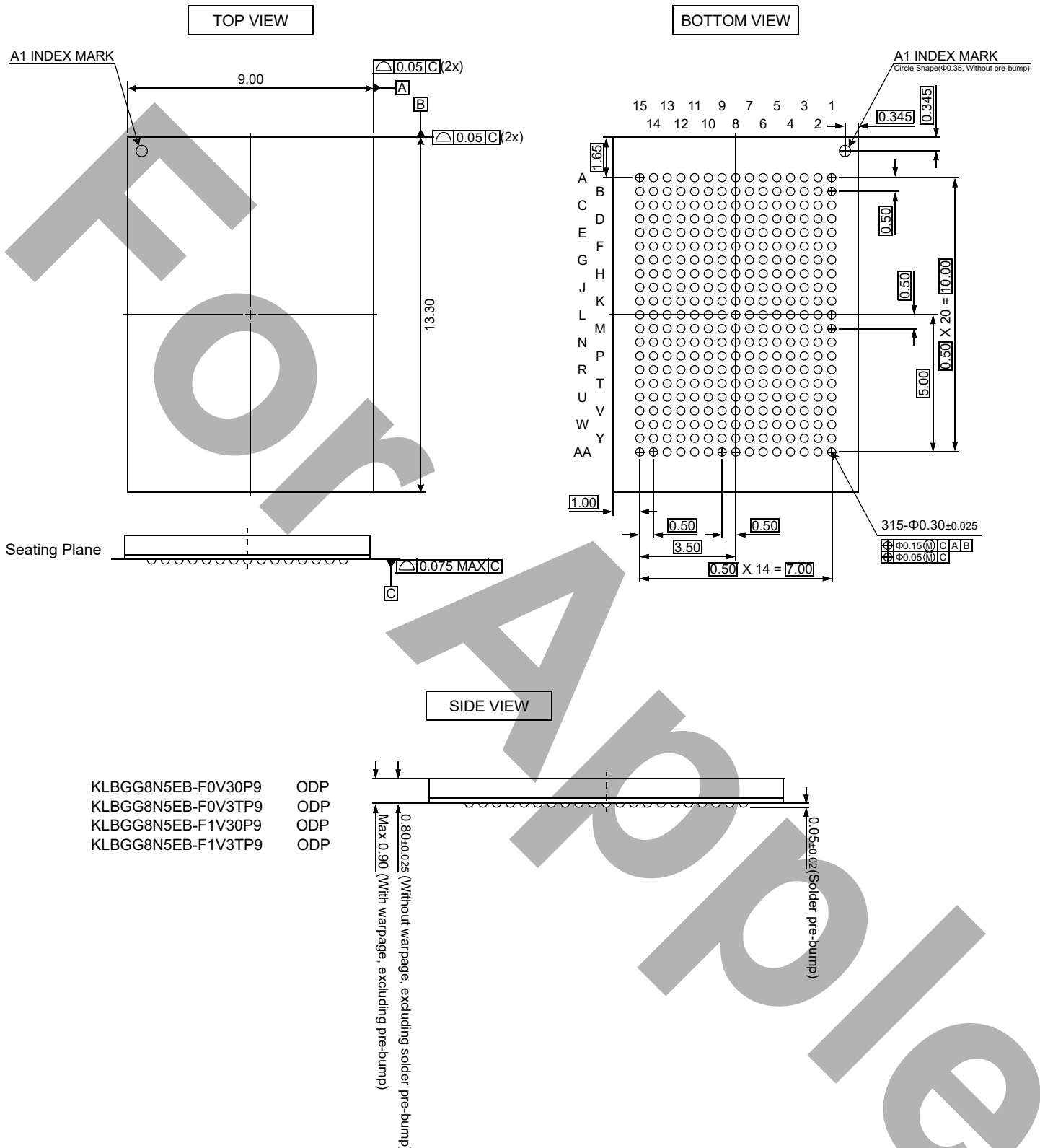
2.2.1.1 S6E Package Size



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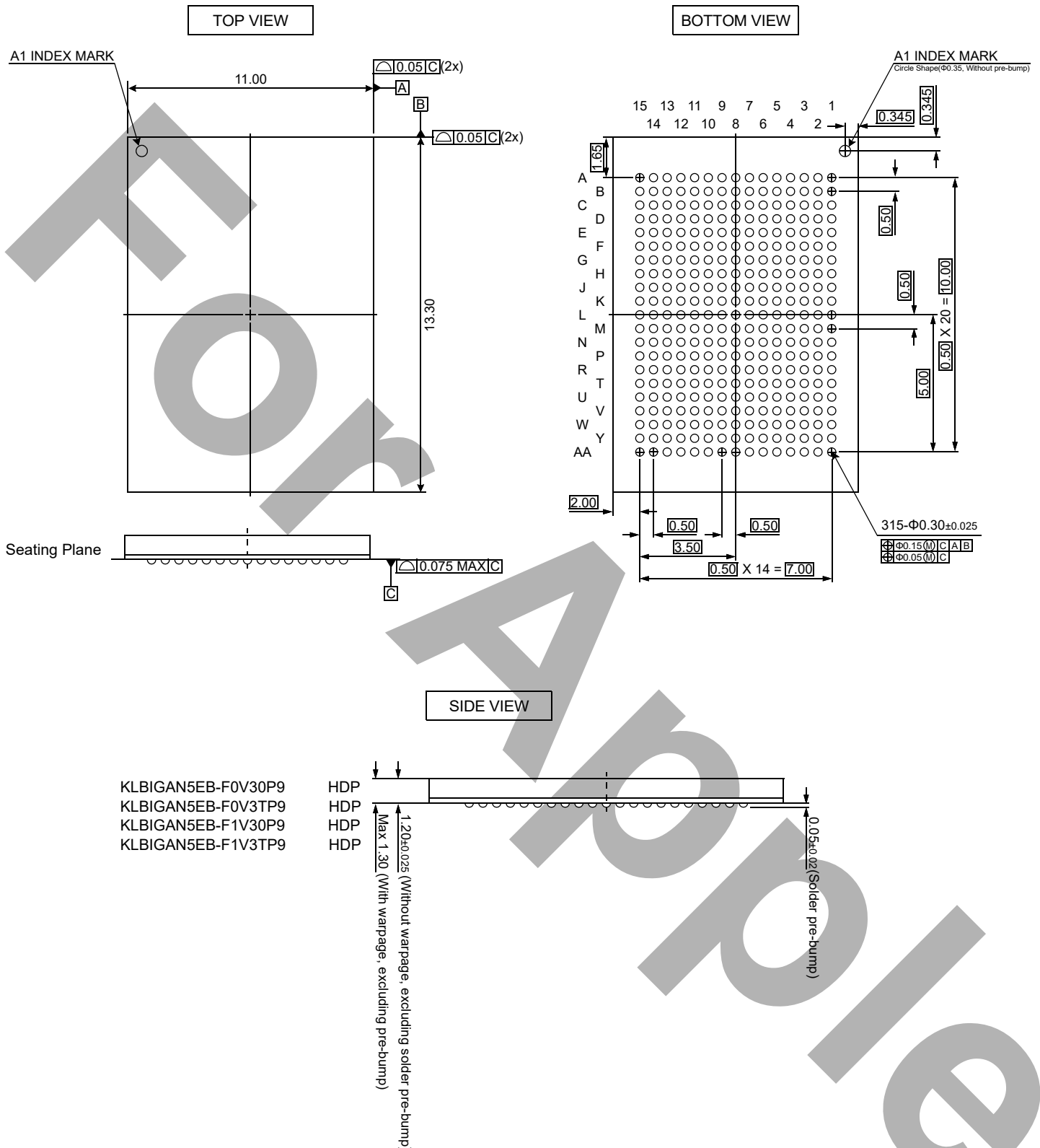
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The S6E package dimensions (X, Y, Body THK Norminal / Z Max including warpage and excluding pre-bump) for shielded.

Part Number	S6E CTRL	APN	Capacity	X (mm)	Y (mm)	Z (mm)	Body THK
KLBDG1N5EB-F0V30P9 KLBDG1N5EB-F0V3TP9	A0	335S00699	1 die	13.3	9	0.75 ¹⁾	0.65
KLBDG1N5EB-F1V30P9 KLBDG1N5EB-F1V3TP9	A1						
KLBEG2N5EB-F0V30P9 KLBEG2N5EB-F0V3TP9	A0	335S00683	2 die	13.3	9	0.75 ¹⁾	0.65
KLBEG2N5EB-F1V30P9 KLBEG2N5EB-F1V3TP9	A1						
KLBFG4N5EB-F0V30P9 KLBFG4N5EB-F0V3TP9	A0	335S00684	4 die	13.3	9	0.75 ¹⁾	0.65
KLBFG4N5EB-F1V30P9 KLBFG4N5EB-F1V3TP9	A1						
KLBGG8N5EB-F0V30P9 KLBGG8N5EB-F0V3TP9	A0	335S00685	8 die	13.3	9	0.9 ²⁾	0.8
KLBGG8N5EB-F1V30P9 KLBGG8N5EB-F1V3TP9	A1						
KLBIGAN5EB-F0V30P9 KLBIGAN5EB-F0V3TP9	A0	335S00686	16 die	13.3	11.0	1.3 ³⁾	1.2
KLBIGAN5EB-F1V30P9 KLBIGAN5EB-F1V3TP9	A1						

NOTE :

- 1) Max Z(THK) is 0.75mm (including warpage and excluding solder pre-bump).
- 2) Max Z(THK) is 0.9mm (including warpage and excluding pre-bump).
- 3) Max Z(THK) is 1.3mm (including warpage and excluding pre-bump).

2.3 Pin Description

This section contains a table with names, direction and functionality description of all external pins.

[Table 2] S6E Signal Description (TBD)

Pin Name	Pin Function
VDDIO_2_L_ANI	NAND interface IO supply
VDDIO_2_DP	NAND interface IO supply
VDDIO_1	External interface supply
PCIE_AVDD_H	PCIE voltage supply
AVDD12_PLL	PLL voltage supply
VQPS	Fuse burning supply (Only). Otherwise, connect to VSS
PCIE_VDD	PCIE digital supply
VDD_PLL	PLL digital supply
VDD	Core digital supply
VCC	Power supply to the NAND array (Not connected to controller)
VPP	NAND supply (Not connected to controller)
VSS	Global chip ground
PCIE_CLKREQ_L	PCie clock request. Active low.
PCIE_TX0_P	Differential TX lane 0
PCIE_TX0_N	
PCIE_RX0_P	Differential RX lane 0
PCIE_RX0_N	
PCIE_REFCLK_P	Differential PCie PHY reference clock
PCIE_REFCLK_N	
PCIE_TSTREF	Test pin for internal use
CLK_IN	24MHz reference clock
RESET_L	Power-On-Reset and global reset, active low
ZQ_0	ANI0 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
ZQ_1	ANI1 controller & NAND_ZQ calibration. Use an on-board 300Ω pull-down.
WP_L	Write_Protect_L – Pin connected to NAND only
DROOP_L	DROOP_L – Proprietary use. Name remains for board compatibility reasons
EXT_D7\ SPF_L	EXT_D7 in HW_BYPASS mode. The host channel 7 th -bit, bidirectional port for transferring address, command, and data to and from the device SPF_L – Sudden Power Fail notification
EXT_D6\ BOOT3	EXT_D6 in HW_BYPASS mode. The host channel 6 th -bit, bidirectional port for transferring address, command, and data to and from the device Bootstrap3 – Input enabled by default- for SW read.
EXT_D5\ SPINAND_MOSI\ SPI_MOSI\ SWD_UID1	EXT_D5 in HW_BYPASS mode. The host channel 5 th -bit, bidirectional port for transferring address, command, and data to and from the device. SPINAND_MOSI – SPI_MOSI pin in SPINAND mode SPI_MOSI – SPI_MOSI pin in SPI mode SWD_UID1 - Proprietary GPIO Unique ID1
EXT_D4\ SPI_CS	EXT_D4 in HW_BYPASS mode. The host channel 4 th -bit, bidirectional port for transferring address, command, and data to and from the device. SPI_CS – SPI Chip Select
EXT_D3\ SPINAND_MISO\ SPI_MISO\ SWD_UID0	EXT_D3 in HW_BYPASS mode. The host channel 3 rd -bit, bidirectional port for transferring address, command, and data to and from the device. SPINAND_MISO – SPI_MISO pin in SPINAND mode SPI_MISO – SPI_MISO pin in SPI mode SWD_UID0 - Proprietary GPIO Unique ID0

EXT_D2\ BOOT2\ SPINAND_SCLK\ SPI_SCLK	EXT_D2 in HW_BYPASS mode. The host channel 2 nd -bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap2 – Input enabled by default- for SW read. SPINAND_SCLK – SPI_SCLK pin in SPINAND mode SPI_SCLK – SPI_SCLK pin in SPI mode
EXT_D1\ BOOT1	EXT_D1 in HW_BYPASS mode. The host channel 1 st -bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap1 – Input enabled by default- for SW read. GPIO – GPIO used as proprietary FW indication
EXT_D0\ BOOT0	EXT_D0 in HW_BYPASS mode. The host channel 0th-bit, bidirectional port for transferring address, command, and data to and from the device. Bootstrap0 – Input enabled by default- for SW read.
EXT_DQS\ BCM	EXT_DQS in HW_BYPASS (DDR) mode. The data strobe signal that indicates the data valid window for the source synchronous data interface. Complementary signal is not in use. Pad disabled in bypass SDR mode BCM (Backward Compatibility Mode) bootstrap
EXT_NCE\ PERST_L	EXT_NCE in HW_BYPASS mode. The Chip Enable signal selects the target. When the Chip Enable is high and the target is in the Normal Ready mode, the target goes into an IDLE mode. When Chip Enable is low, the target is selected. PERST_L ? In functional mode, PCIe side reset event. SW handled.
EXT_RnB\ JTAG_TDO	EXT_RnB in HW_BYPASS mode. Ready/Busy signal indicates the device status when the device executes legacy commands (read, erase, program and reset). When low, the signal indicates that one or more operations are in progress. JTAG_TDO – JTAG Test Data Out bit
EXT_NRE\ JTAG_TMS	EXT_NRE in HW_BYPASS mode. The Read Enable signal enables data output. JTAG_TMS – JTAG Test Mode Select bit
EXT_ALE\ JTAG_SEL	EXT_ALE in HW_BYPASS mode. The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). JTAG_SEL – JTAG Select bit
EXT_CLE\ JTAG_TDI	EXT_CLE in HW_BYPASS mode. The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). JTAG_TDI – JTAG Test Data In bit
EXT_NWE\ JTAG_TCK	EXT_NWE in HW_BYPASS mode. The Write Enable signal controls the latching of input data in the asynchronous data interface. Data, commands, and addresses are latched on the rising edge of WE#. JTAG_TCK – JTAG Clock bit
JTAG_TRSTN	JTAG_TRSTN – JTAG Test RESETN.
RFU[10:0]	RFU bus in Mini/Micro packages
RFU2[15:0]	RFU2 bus in Mini/Micro packages
MGND[130:0]	Mechanical ground pins in Mini/Micro packages
ONC	Orientation No Connection in Mini/Micro packages
VSF[3:0]	Vendor Specific Function