128/256/512/1024GB E3NAND

128GB : HN3T0HT1DAX430

256GB : HN3T1HT2DAX430

512GB : HN3T2HT4DAX431

1024GB : HN3T3HT8DAX432

2048GB : HN3T4HTGDAX433

Document Title
128/256/512/1024/2048GB E3NAND Specification

Revision History

Table1. Document Revision History

Revision No.	History	Draft Date
0.0	-. Draft version	Feb. 07. 2024
0.1	-. 16DP updated	Feb. 15. 2024

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1. Introduction

1.1. Goals and Objectives

This document communicates the specification for E3NAND

1.2. Key Features

■ **Physical Interface**
- PCIe Gen5

■ **Memory Technology**
- 1Tb 3bit per cell

■ **E3NAND Organization**
- 128GB : 1+1-stacks
- 256GB : 1+2-stacks
- 512GB : 1+4-stacks
- 1024GB : 1+8-stacks
- 2048GB : 1+16-stacks

■ **Power Supply**
- VDD for high VDD operational mode : TBD
- VDD for low VDD operational mode : TBD
- VCCQ for high VCCQ operational mode : TBD
- VCCQ for low VCCQ operational mode : TBD
- VCC : TBD

■ **Net Weight**
- 128GB : TBD [g]
- 256GB : TBD [g]
- 512GB : TBD [g]
- 1024GB : TBD [g]
- 2048GB : TBD [g]

■ **Package**
- 128/256/512GB : LGA315 (09.0 x 13.3 X 0.75mm)
- 1024GB : LGA315 (09.0 x 13.3 X 0.9mm)
- 2048GB : LGA315 (11.0 x 13.3 X 0.9mm)

■ **FW version**
- TBD

■ **E3NAND controller version**
- S6E (TBD)

■ **Operation Temp**
- Case surface temperature (-25~100C)

1.3. Product List

1.3.1. Part number

Part Number	VDD	VDDIO	VCC	Organization	Density	B/E site
HN3T0HT1DAX430	TBD	TBD	TBD	1 + 1	128GB	CJ
HN3T1HT2DAX430	TBD	TBD	TBD	1 + 2	256GB	CJ
HN3T2HT4DAX431	TBD	TBD	TBD	1 + 4	512GB	CJ
HN3T3HT8DAX432	TBD	TBD	TBD	1 + 8	1024GB	CJ
HN3T4HTGDAX433	TBD	TBD	TBD	1 + 16	2048GB	CJ

1.3.2. Marking Information

No		Code	
1	H	SK hynix	SK hynix
2	N	Product Family	Flash
3	3	Product Mode	Customized
4,5	G9 T0 T1 GQ GS T2 GV GT T3 T4	Product Density	G9 : 64GB T0 : 128GB GP : 192GB T1 : 256GB GQ : 320GB GS : 384GB T2 : 512GB GV : 576GB GT : 640GB T3 : 1TB T4 : 2TB
6	8 9 A B C D E F H	NAND Info	8 : 3DV4 256G 9 : 3DV4 512G A : 3DV5 512G B : 3DV6 512G C : 3DV6 1T D : 3DV7 512G F : 3DV8 512G H : 3DV9 1T
7	T	Cell Type	TLC
8	1 2 3 4 5 6 8 9 A G	Number of Die	1 : SDP 2 : DDP 3 : TDP 4 : QDP 5 : 5DP 6 : 6DP 8 : ODP 9 : 9DP A : 10DP G : 16DP
9	A B C D	Controller Name	A : S3E B : S4E C : S5E D : S6E
10	A	Client Name	Apple
11	X	Reserved	
12	Combination Code		
13			
14			

2. Physical Interface

2.1. Package Pin Layout

The S6E LGA has 315 pins, with the pin list and layout as shown below

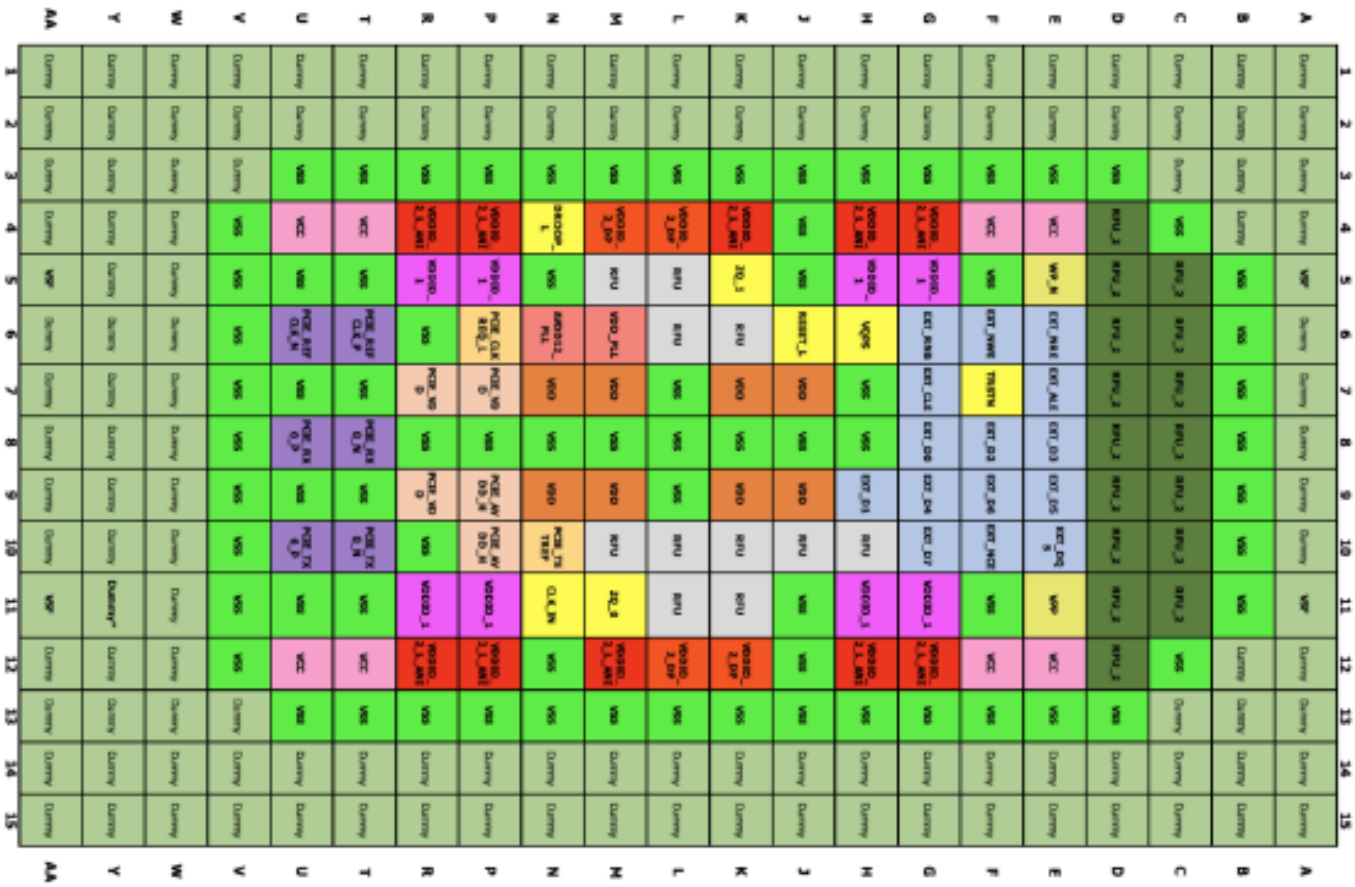
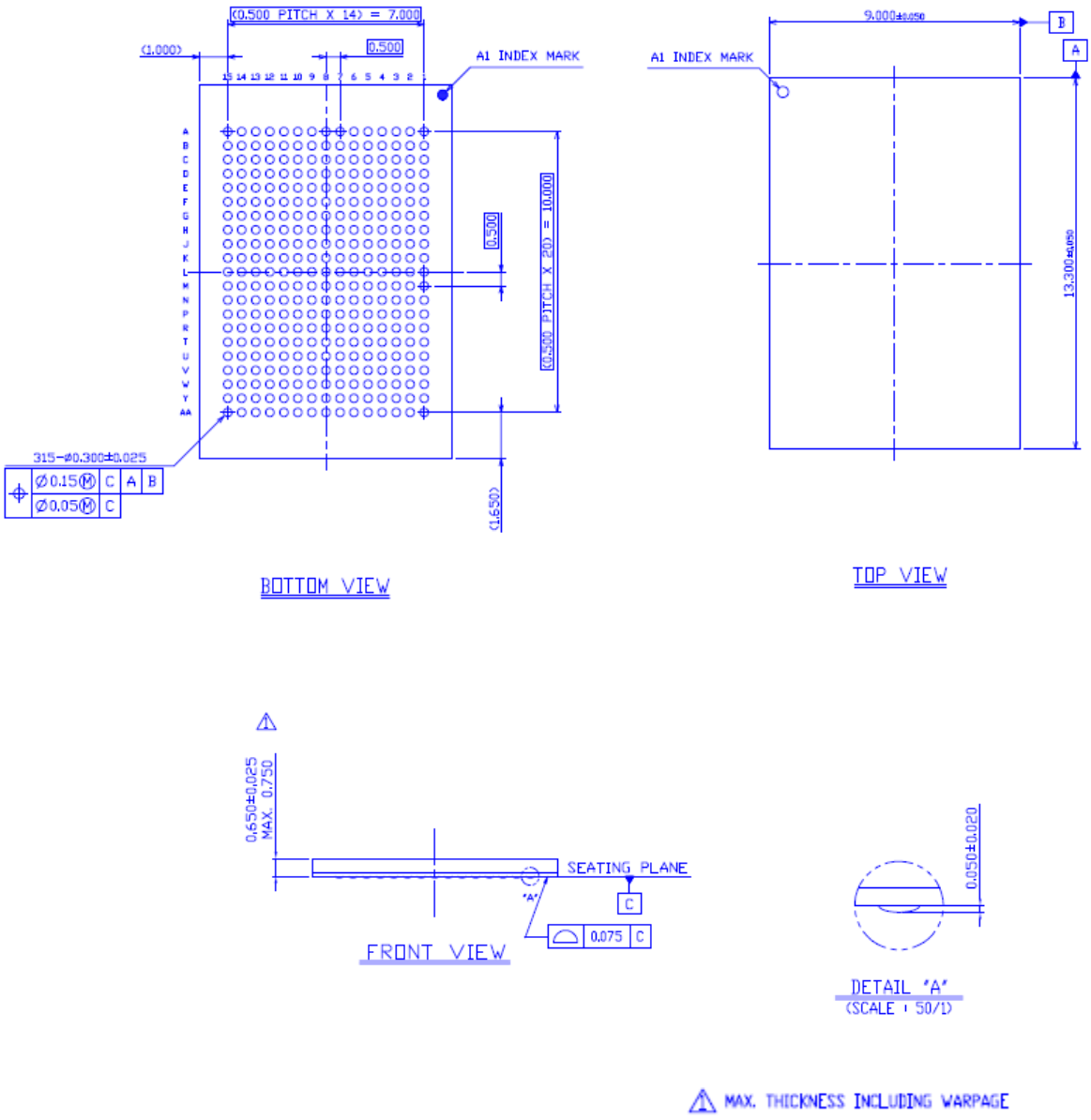


Figure 1: S6E Package LGA315 Pin Assignment

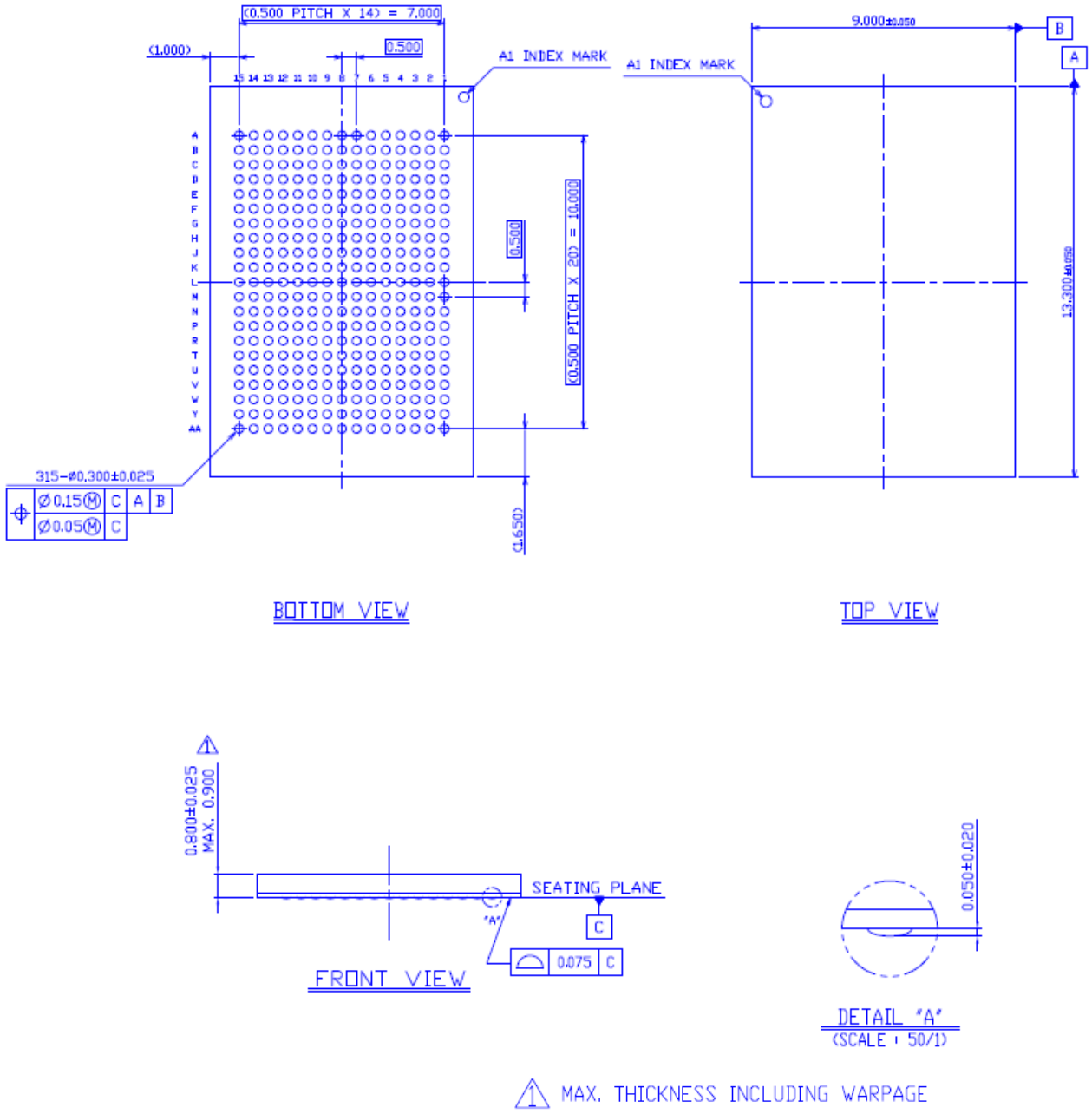
Package Pins	Usage in package	Comment
VDDIO_2_L_ANI	Same as VDDIO_2	NAND IF IO supply
VDDIO_2_DP	Same as VDDIO_2 Merged with VDDIO_2_L_ANI	Included in VDDIO_2_L_ANI for SIPI purpose *May separate beyond S6E package
RFU	Floating individually	Reserved for Future Use
RFU_2	Floating individually	Reserved for Future Use
Dummy	Tied to VSS	
Dummy*	Floating	*Y11 pin
VSF	- If vendor doesn't use VSF, these pins shall be shorted to VSS in package substrate - If vendor implement VSF connection to NAND die(s), 1. Vendor shall provide pre-notification and function of the pins to Apple, and need Apple approval before implementation 2. These pins in NAND die user mode shall be self-pulldown to VSS, or shall keep stable high-Z with characteristics confirmed with Apple 3. These pins in NAND die user mode shall be allowed to float or short to VSS, in Apple side usage 4. These pins also shall comply with ESD specifications	Vendor Specific Feature *A5, A11, AA5, AA11 pins

Table 2: Usage of VDDIO_2_L_ANI, VDDIO_2_DP, RFU, RFU_2, Dummy, Dummy* and VSF pins

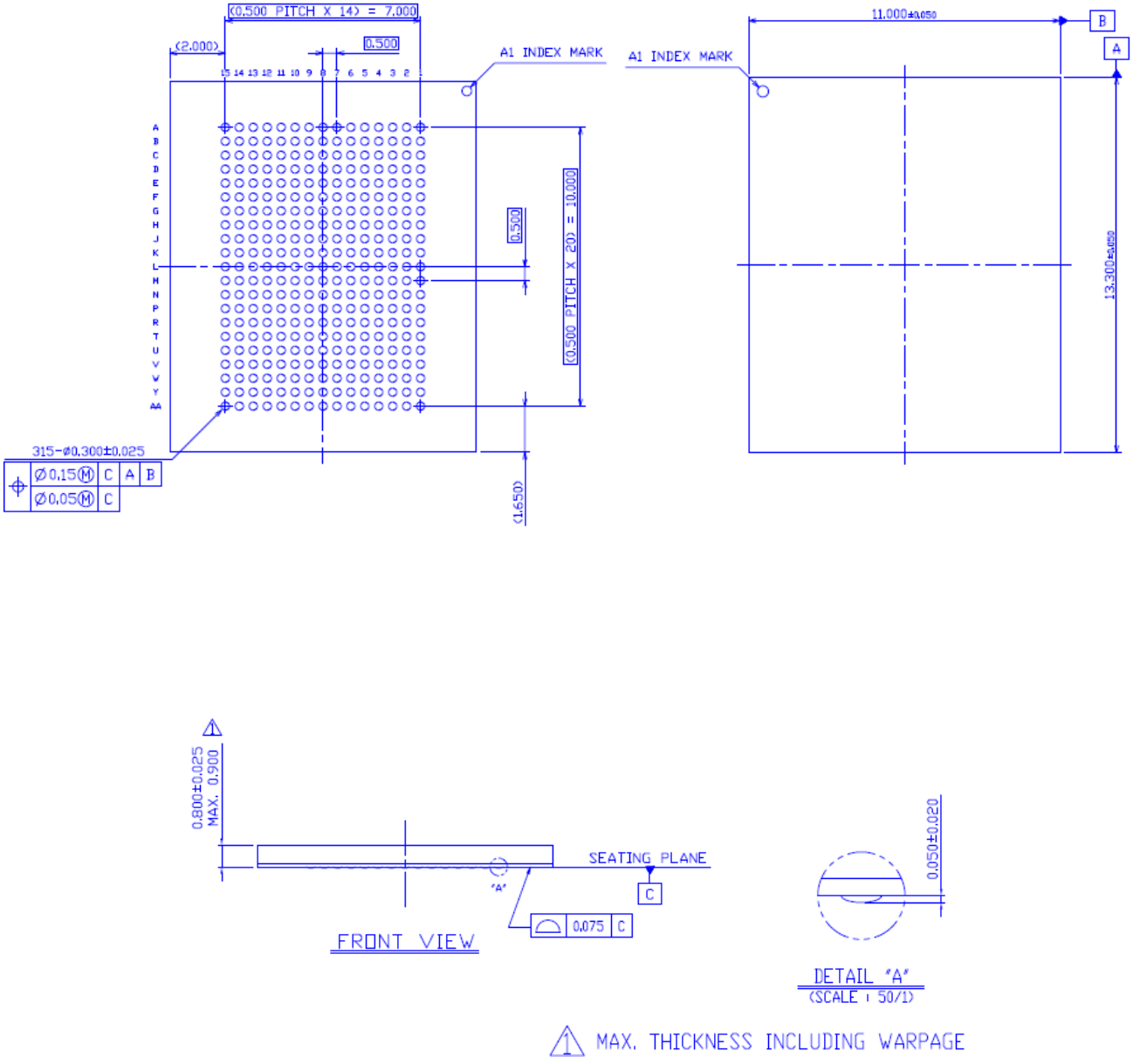
Number of NAND stack	X (mm)	Y (mm)	Z max (mm)	Body THK (mm)	Pre-bump (㎛)
1 / 2 / 4 die	13.3 (±0.05)	9.0 (±0.05)	0.75	0.65 (±0.025)	50 (±20)
8 die	13.3 (±0.05)	9.0 (±0.05)	0.9	0.8 (±0.025)	
16 die	13.3 (±0.05)	11.0 (±0.05)			



13.3x9.0x0.75mm LGA315 Package Outline Drawing



13.3x9.0x0.9mm LGA315 Package Outline Drawing



13.3x11.0x0.9mm LGA315 Package Outline Drawing